74HCT221

Dual non-retriggerable monostable multivibrator with reset

Rev. 3 — 26 October 2016 **Product data sheet**

1. General description

The 74HCT221 is a dual non-retriggerable monostable multivibrator. Each multivibrator features edge-triggered inputs ($n\overline{A}$ and nB), either of which can be used as an enable input. Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry for the nB inputs allow jitter-free triggering from inputs with slow transition rates, providing the circuit with excellent noise immunity. Once triggered, the outputs (nQ, $n\overline{Q}$) are independent of further transitions of $n\overline{A}$ and nB inputs. The output pulse width is defined by the following relationship: $t_W = 0.7 \times C_{EXT} \times R_{EXT}$ The output pulses can be terminated by the active LOW reset inputs ($n\overline{RD}$). Pulse width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications pulse stability will only be limited by the accuracy of the external timing components. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Input levels:
  - For 74HCT221: TTL level
- Pulse width variance is typically less than ±5%
- Direct reset terminates output pulse
- Schmitt-trigger action on nB inputs
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HCT221D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

nexperia

4. Functional diagram

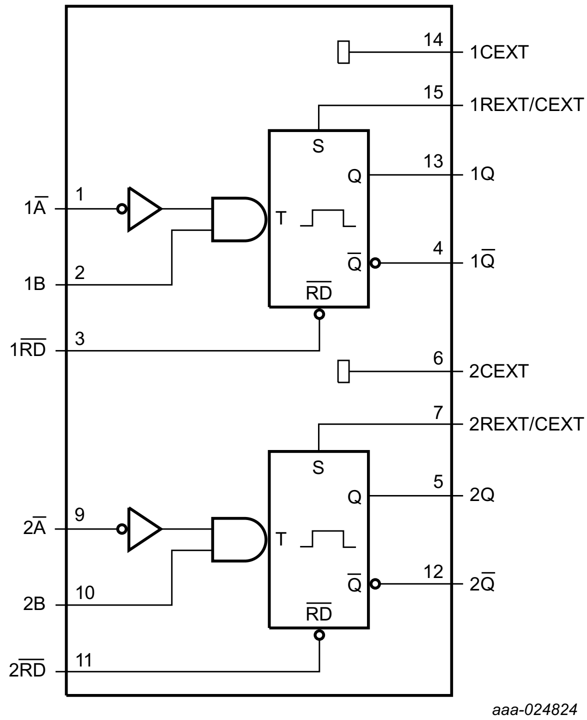


Fig 1. Functional diagram

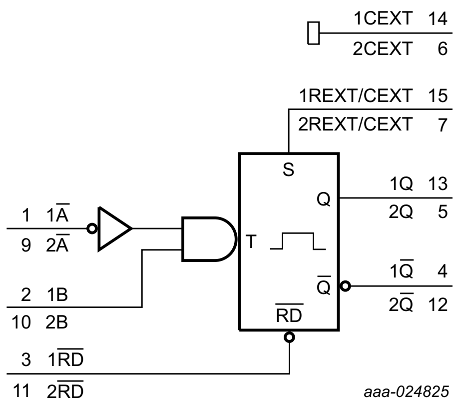


Fig 2. Logic symbol

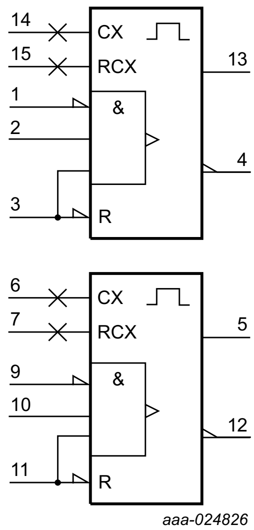


Fig 3. IEC logic symbol

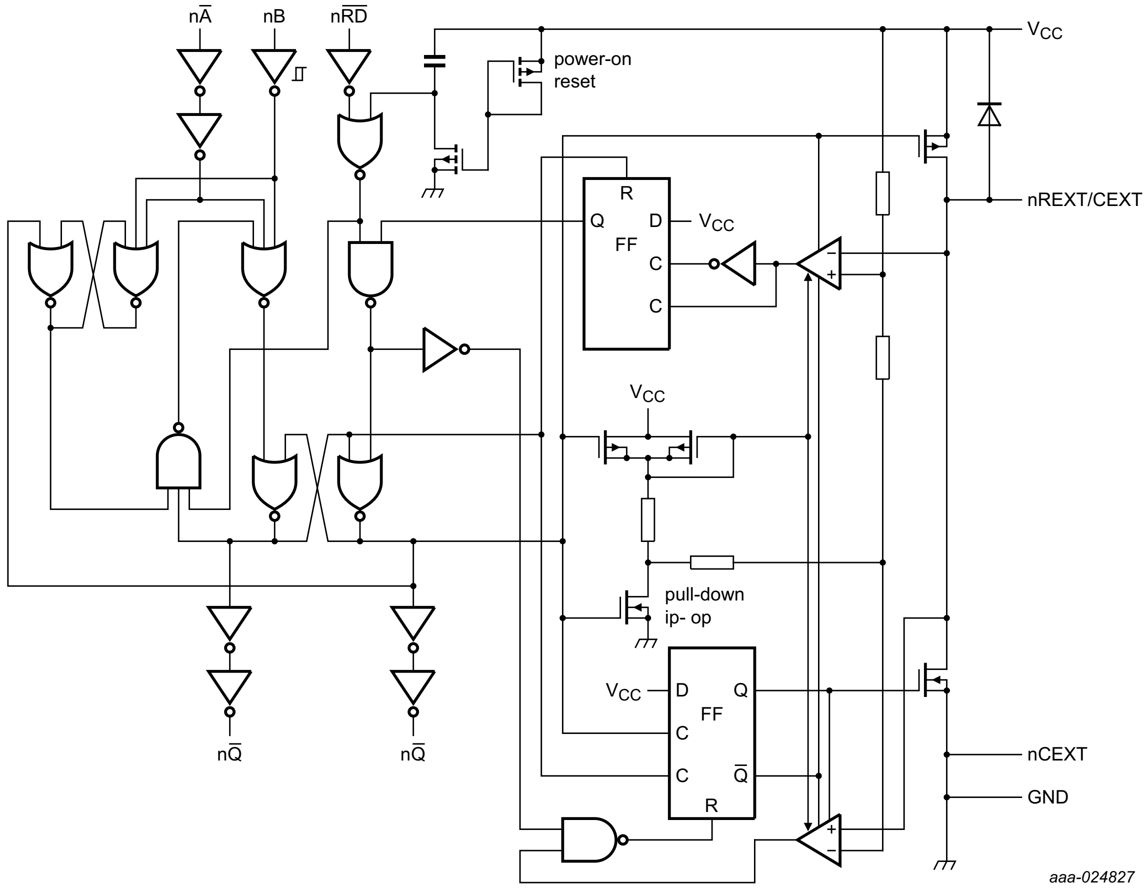
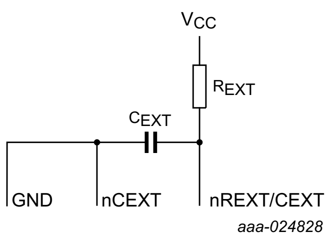


Fig 4. Logic diagram



It is recommended to connect pins nCEXT externally to the GND pin.

Fig 5. Timing component connections

5. Pinning information

5.1 Pinning

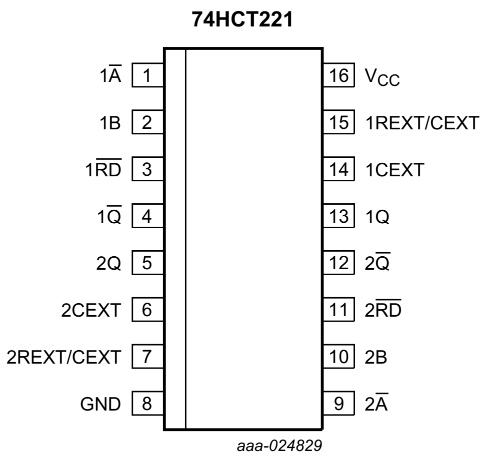


Fig 6. Pin configuration for SO16

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$1\overline{A}$	1	negative-edge triggered input 1
1B	2	positive-edge triggered input 1
$1\overline{RD}$	3	direct reset LOW and positive-edge triggered input 1
$1\overline{Q}$	4	active LOW output 1
2Q	5	active HIGH output 2
2CEXT	6	external capacitor connection 2
2REXT/CEXT	7	external resistor and capacitor connection 2
GND	8	ground (0 V)
$2\overline{A}$	9	negative-edge triggered input 2
2B	10	positive-edge triggered input 2
$2\overline{RD}$	11	direct reset LOW and positive-edge triggered input 2
$2\overline{Q}$	12	active LOW output 2
1Q	13	active HIGH output 1
1CEXT	14	external capacitor connection 1
1REXT/CEXT	15	external resistor and capacitor connection 1
V_{CC}	16	supply voltage

6. Functional description

Table 3. Function table[1]

Input			Output	
$n\overline{RD}$	$n\overline{A}$	nB	nQ	$n\overline{Q}$
L	X	X	L	H
X	H	X	L[2]	H[2]
X	X	L	L[2]	H[2]
H	L	↑	⊓	⊔
H	↓	H	⊓	⊔
↑	L	H	⊓ [3]	⊔ [3]

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = LOW-to-HIGH transition; ↓ = HIGH-to-LOW transition;

⊓ = one HIGH level output pulse; ⊔ = one LOW level output pulse.

[2] If the monostable was triggered before this condition was established, the pulse will continue as programmed.

[3] For this combination the reset input must be LOW and the following sequence must be used:
pin $n\overline{A}$ must be set HIGH or pin nB set LOW; then pin $n\overline{A}$ must be LOW and pin nB set HIGH. Now the reset input goes from LOW-to-HIGH and the device will be triggered.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	-	±20	mA
I_O	output current	except for pins nREXT/CEXT; $V_O = -0.5$ V to (V_{CC} + 0.5 V)	-	±25	mA
I_{CC}	supply current		-	50	mA
I_{GND}	ground current		–50	-	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	total power dissipation	SO16 package [1]	-	500	mW

[1] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
$\Delta t/\Delta V$	input transition rise and fall rate	nA, $n\overline{RD}$ input				
		V_{CC} = 4.5 V	-	1.67	139	ns/V
T_{amb}	ambient temperature		–40	+25	+125	°C

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V								
		I_O = –20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = –4 mA	3.98	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V								
		I_O = 20 μA	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA	-	0.15	0.26	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	8.0	-	80	-	160	μA
ΔI_{CC}	additional supply current	per input pin; I_O = 0 A; $V_I = V_{CC} - 2.1$ V; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V								
		pin nB	-	30	108	-	135	-	147	μA
		pins $n\overline{A}$, $n\overline{RD}$	-	50	180	-	225	-	245	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Figure 15.

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	LOW to HIGH propagation delay	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; see Figure 7 and Figure 8								
		$n\overline{A}$, $n\overline{RD}$ to nQ (trigger)								
		V_{CC} = 4.5 V	-	30	50	-	63	-	75	ns
		V_{CC} = 5 V; C_L = 15 pF	-	36	-	-	-	-	-	ns
		nB to nQ (trigger)								
		V_{CC} = 4.5 V	-	24	42	-	53	-	63	ns
		V_{CC} = 5 V; C_L = 15 pF	-	36	-	-	-	-	-	ns
		$n\overline{RD}$ to $n\overline{Q}$ (reset)								
		V_{CC} = 4.5 V	-	31	51	-	64	-	77	ns
		V_{CC} = 5 V; C_L = 15 pF	-	36	-	-	-	-	-	ns
t_{PHL}	HIGH to LOW propagation delay	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; see Figure 7 and Figure 8								
		$n\overline{A}$ to $n\overline{Q}$ (trigger)								
		V_{CC} = 4.5 V	-	26	44	-	55	-	75	ns
		V_{CC} = 5 V; C_L = 15 pF	-	32	-	-	-	-	-	ns
		nB to $n\overline{Q}$ (trigger)								
		V_{CC} = 4.5 V	-	21	35	-	44	-	53	ns
		V_{CC} = 5 V; C_L = 15 pF	-	32	-	-	-	-	-	ns
		$n\overline{RD}$ to $n\overline{Q}$ (trigger)								
		V_{CC} = 4.5 V	-	26	43	-	54	-	65	ns
		V_{CC} = 5 V; C_L = 15 pF	-	32	-	-	-	-	-	ns
		$n\overline{RD}$ to nQ (reset)								
		V_{CC} = 4.5 V	-	26	43	-	54	-	65	ns
		V_{CC} = 5 V; C_L = 15 pF	-	32	-	-	-	-	-	ns
t_t	transition time	V_{CC} = 4.5 V; see Figure 7 [1]	-	7	15	-	19	-	22	ns

Table 7. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Figure 15.

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_W	pulse width	n$\overline{A}$ LOW; nB HIGH; (trigger); see Figure 7								
		V_{CC} = 4.5 V	20	13	-	25	-	30	-	ns
		n$\overline{RD}$ LOW; see Figure 10								
		V_{CC} = 4.5 V	22	13	-	28	-	33	-	ns
		nQ HIGH and n$\overline{Q}$ LOW; see Figure 8								
		V_{CC} = 5 V; C_{EXT} = 100 nF; R_{EXT} = 10 kΩ	630	700	770	602	798	595	805	µs
		nQ or n$\overline{Q}$ (trigger); see Figure 8								
		V_{CC} = 4.5 V; C_{EXT} = 28 pF; R_{EXT} = 2 kΩ	-	140	-	-	-	-	-	ns
		V_{CC} = 4.5 V; C_{EXT} = 1 nF; R_{EXT} = 2 kΩ	-	1.5	-	-	-	-	-	µs
		V_{CC} = 4.5 V; C_{EXT} = 1 nF; R_{EXT} = 10 kΩ	-	7	-	-	-	-	-	µs
t_{rec}	recovery time	n$\overline{RD}$ to n$\overline{A}$, nB; see Figure 11	20	12	-	25	-	30	-	ns
R_{EXT}	external timing resistor	V_{CC} = 5.0 V; see Figure 13	2	-	1000	-	-	-	-	kΩ
C_{EXT}	external timing capacitor	V_{CC} = 5.0 V; see Figure 13	no limits							pF

Table 7. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Figure 15.

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
C_{PD}	power dissipation capacitance	per monostable; V_I = GND to V_{CC} − 1.5 V [2]	-	96	-	-	-	-	-	pF

[1] t_t is the same as t_{THL} and t_{TLH}

[2] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o) + 0.33 \times C_{EXT} \times V_{CC}^2 \times f_o + D \times 28 \times V_{CC}$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

D = duty factor in %;

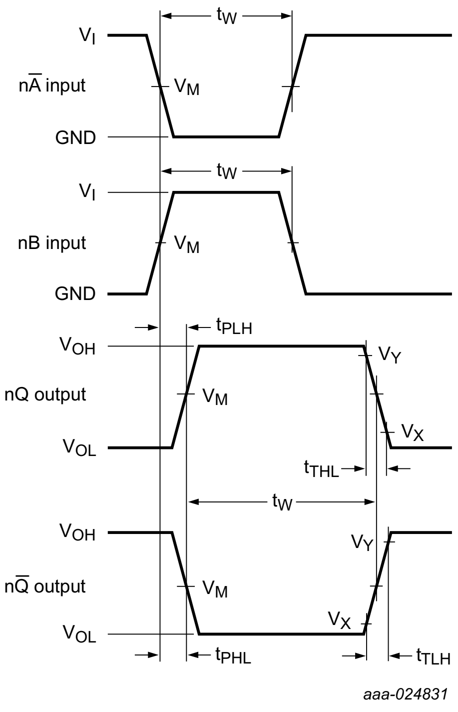
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

C_{EXT} = timing capacitance in pF;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ sum of outputs.

11. Waveforms and graphs



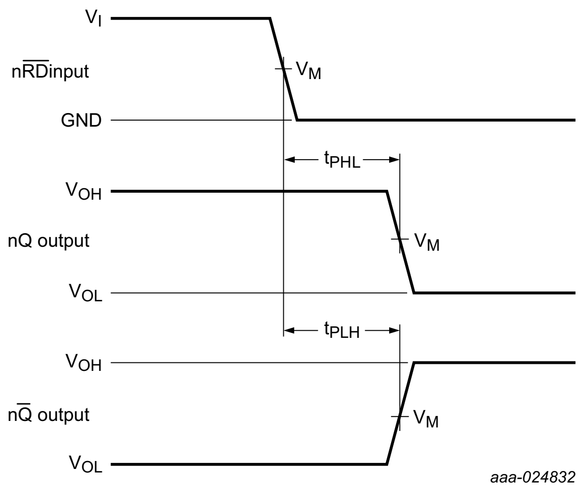
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 7. Propagation delay from input ($n\overline{A}$, nB) to output (nQ, $n\overline{Q}$), $n\overline{A}$, nB pulse widths and output transition times

Table 8. Measurement points

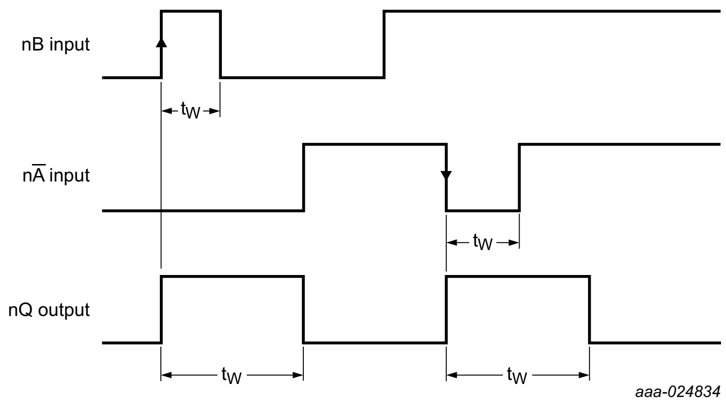
Input	Output		
V_M	V_M	V_X	V_Y
1.3 V	1.3 V	$0.1V_{CC}$	$0.9V_{CC}$



Measurement points are given in Table 8.

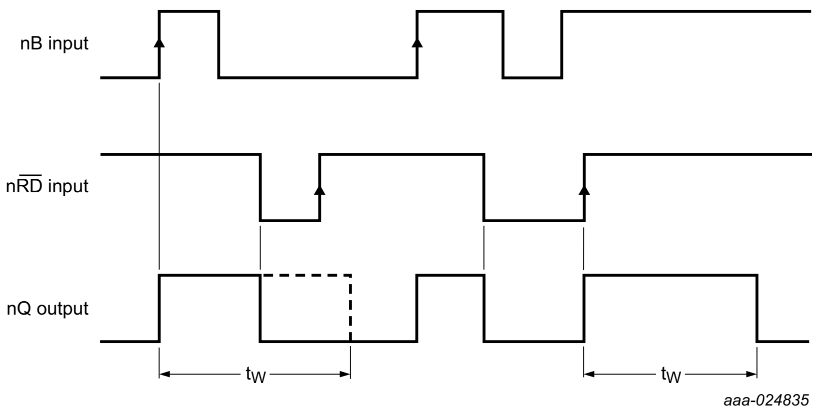
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 8. Propagation delay from reset input ($n\overline{RD}$) to outputs (nQ, $n\overline{Q}$)



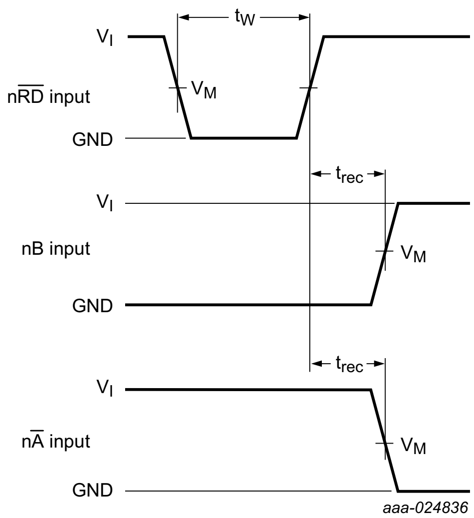
$n\overline{RD}$ = HIGH

Fig 9. Output pulse control



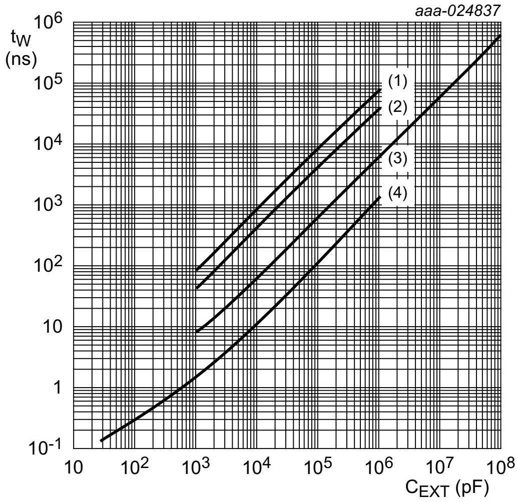
n$\overline{A}$ = LOW

Fig 10. Output pulse control using reset input n$\overline{RD}$



Measurement points are given in Table 8.

Fig 11. Reset input (n$\overline{RD}$) to inputs n$\overline{A}$ or nB recovery times



V_{CC} = 4.5 V; T_{amb} = 25 °C.

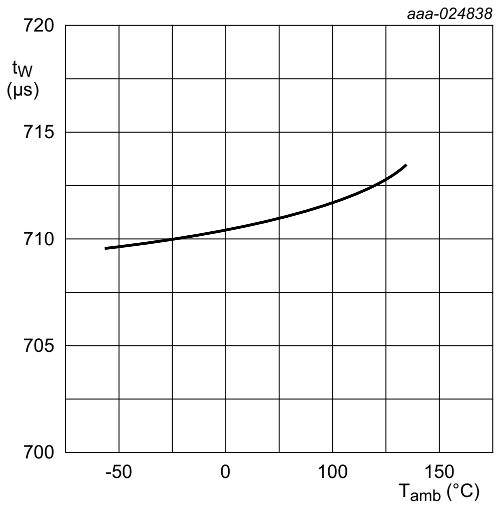
(1) R_{EXT} = 100 kΩ

(2) R_{EXT} = 50 kΩ

(3) R_{EXT} = 10 kΩ

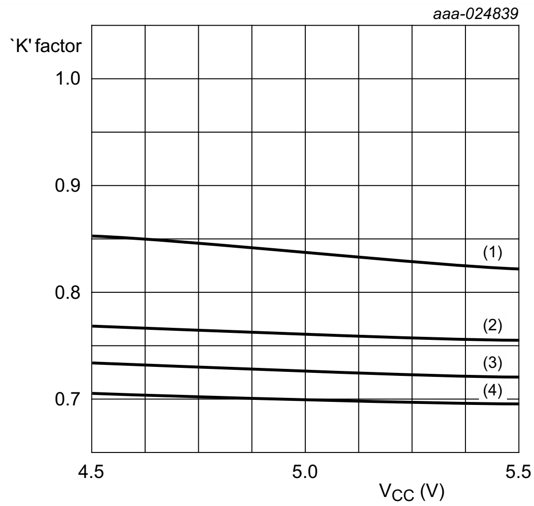
(4) R_{EXT} = 2 kΩ

Fig 12. Typical output pulse width as a function of the external capacitor



C_{EXT} = 0.1 μF; R_{EXT} = 10 kΩ.; V_{CC} = 5.0 V

Fig 13. Typical output pulse width as a function of the ambient temperature



R_{EXT} = 10 kΩ; T_{amb} = 25 °C.

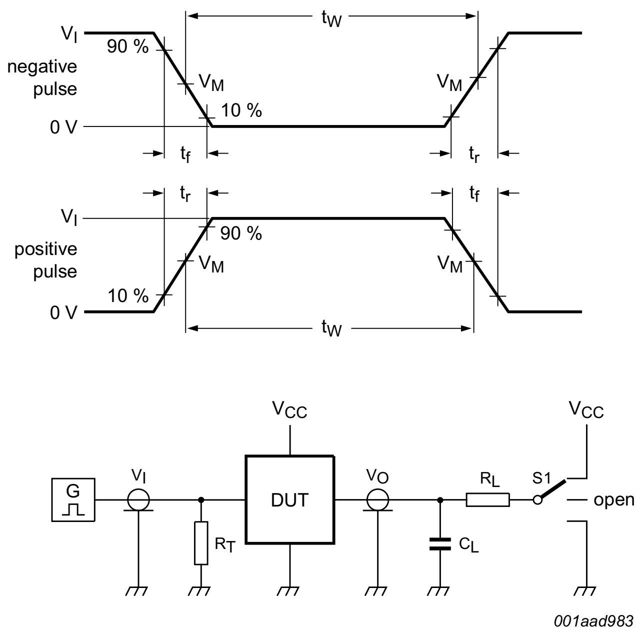
(1) C_{EXT} = 0.001 μF

(2) C_{EXT} = 0.01 μF

(3) C_{EXT} = 0.1 μF

(4) C_{EXT} = 1 μF

Fig 14. “K” factor as function of the supply voltage



Test data is given in Table 9.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch.

Fig 15. Test circuit for measuring switching times

Table 9. Test data

Input		Load		S1 position
V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
3 V	6 ns	15 pF, 50 pF	1 kΩ	open

12. Application information

12.1 Power-down considerations

A large capacitor C_{EXT} may cause problems when powering-down the monostable due to the energy stored in this capacitor. When a system containing this device is powered-down or a rapid decrease of V_{CC} to zero occurs, the monostable may sustain damage, due to the capacitor discharging through the input protection diodes. To avoid this possibility, use a damping diode (D_{EXT}) preferably a germanium or Schottky type diode able to withstand large current surges and connect as shown in Figure 16.

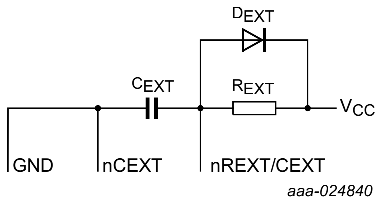
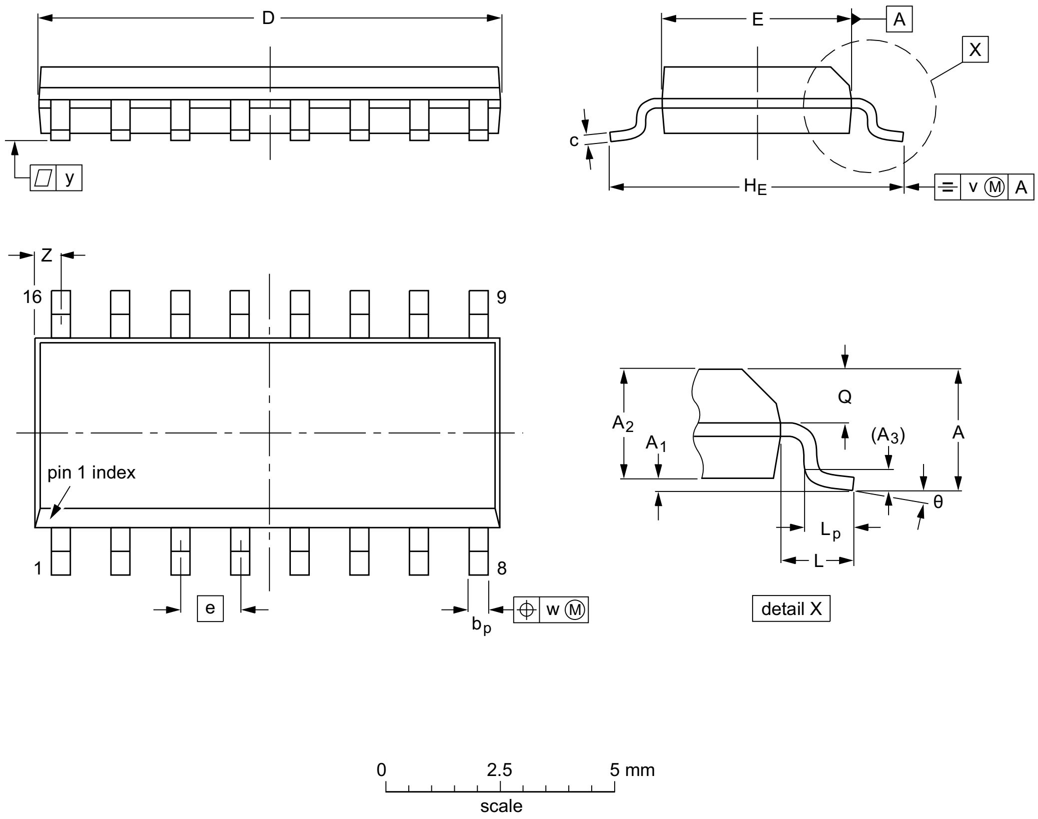


Fig 16. Power-down protection circuit

13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 17. Package outline SOT109-1 (SO16)

14. Abbreviations

Table 10. Abbreviations

Acronym	Abbreviation
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HCT221 v.3	20161026	Product data sheet	-	74HC_HCT221 v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Type numbers 74HC221N, 74HC221D, 74HC221DB and 74HCT221N removed.			
74HC_HCT221 v.2	19901201	Product specification	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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17. Contact information

For more information, please visit: **http://www.nexperia.com**

For sales office addresses, please send an email to: **salesaddresses@nexperia.com**

18. Contents

For more information, please visit: http://www.nexperia.com
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