



ESDALC14V2-2BP5 ESDALC25-2BP5

Low capacitance TRANSIL™ array for ESD protection

Main applications

Where transient overvoltage protection in ESD sensitive equipment is required, such as :

- Computers
- Printers
- Communication systems such as xDSL modem
- Video equipment

This device is particularly adapted to the protection of symmetrical systems

Features

- 2 Bidirectional Transil functions
- Breakdown voltage:
 $V_{BR} = 14.2 \text{ V}$ and 25 V minimum
- Low leakage current: $< 1 \mu\text{A}$
- Low diode capacitance: 14 and 8 pF at 3 V
- Very small PCB area $< 2.6 \text{ mm}^2$

Description

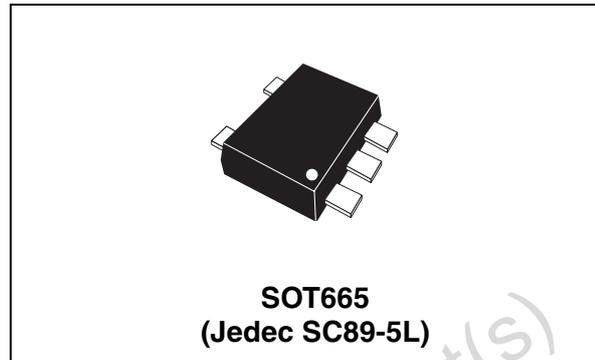
The ESDALCxx-2BP5 is a monolithic array designed to protect up to 2 lines against ESD transients.

The device is ideal for situations where board space saving is required.

Benefits

- High ESD protection level
- High integration
- Suitable for high density boards

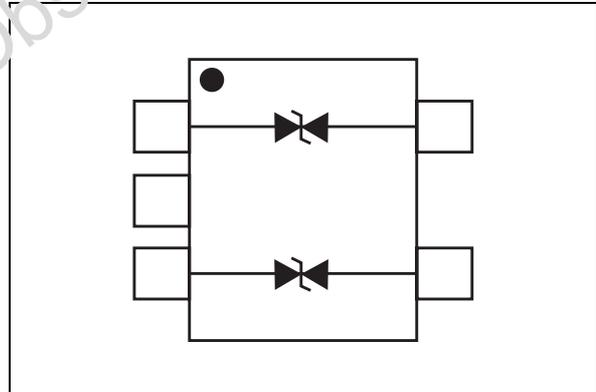
TM: TRANSIL is a trademark of STMicroelectronics



Order codes

| Part Number | Marking |
|-----------------|---------|
| ESDALC14V2-2BP5 | A3 |
| ESDALC25-2BP5 | A4 |

ESDALCxx-2BP5 Functional diagram



Complies with the following standards

IEC61000-4-2

Level 4 15 kV (air discharge)
 8 kV (contact discharge)

MIL STD 883E - Method 3015-7 Class 3

25 kV HBM (Human Body Model)

1 Characteristics

Table 1. Absolute Ratings ($T_{amb} = 25^{\circ}\text{C}$)

| Symbol | Parameter | Value | Unit |
|-----------|---|-------------|--------------------|
| P_{PP} | Peak pulse power (8/20 μs) ⁽¹⁾ | 50 | W |
| T_j | Junction temperature | 150 | $^{\circ}\text{C}$ |
| T_{stg} | Storage temperature range | -55 to +150 | $^{\circ}\text{C}$ |
| T_L | Maximum lead temperature for soldering during 10s | 260 | $^{\circ}\text{C}$ |
| T_{op} | Operating temperature range ⁽²⁾ | -40 to +150 | $^{\circ}\text{C}$ |

1. For a surge greater than the maximum values, the diode will fail in short circuit
2. The values of the operating parameters versus temperature are given through curves and αT parameter.

1.1 Electrical characteristics ($T_{amb} = 25^{\circ}\text{C}$)

| Symbol | Parameter |
|------------|---------------------------------|
| V_{RM} | Stand-off voltage |
| V_{BR} | Breakdown voltage |
| V_{CL} | Clamping voltage |
| I_{RM} | Leakage current |
| I_{PP} | Peak pulse current |
| αT | Voltage temperature coefficient |
| V_F | Forward voltage drop |
| C | Capacitance |
| R_d | Dynamic resistance |

| Part Numbers | $V_{BR} @ I_R$ | | $I_{RM} @ V_{RM}$ | | | R_d | αT | C |
|-----------------|----------------|------|-------------------|---------------|----|----------|----------------------------|-----------------|
| | min. | max. | max. | | | typ. | max. | typ. 3V bias |
| | V | V | mA | μA | V | Ω | $10^{-4}/^{\circ}\text{C}$ | pF |
| ESDALC14V2-2BP5 | 14.2 | 18 | 1 | 1 | 12 | 1.5 | 7 | 14 |
| ESDALC25-2BP5 | 25 | 29.7 | 1 | 1 | 24 | 1.3 | 8 | 8 |

Figure 1. Peak pulse power versus initial junction temperature

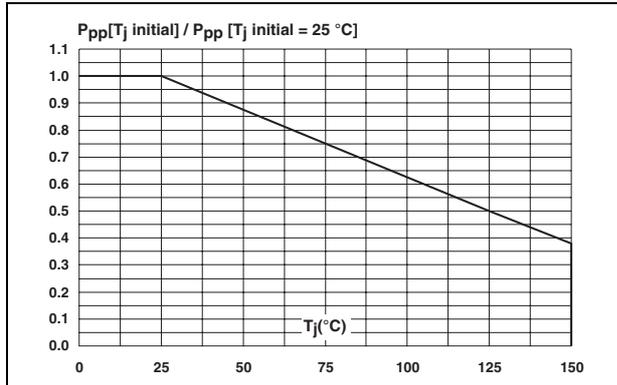


Figure 2. Peak pulse power versus exponential pulse duration

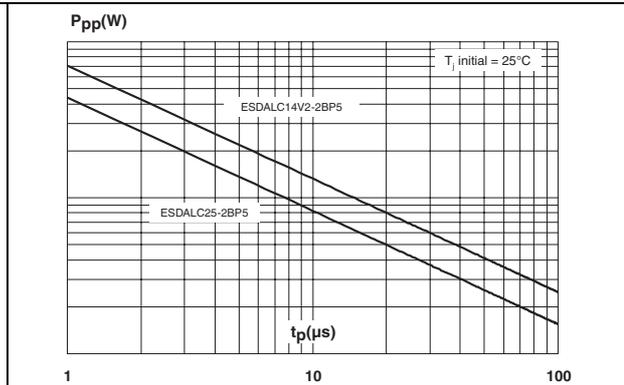


Figure 3. Clamping voltage versus peak pulse current (maximum values, rectangular waveform)

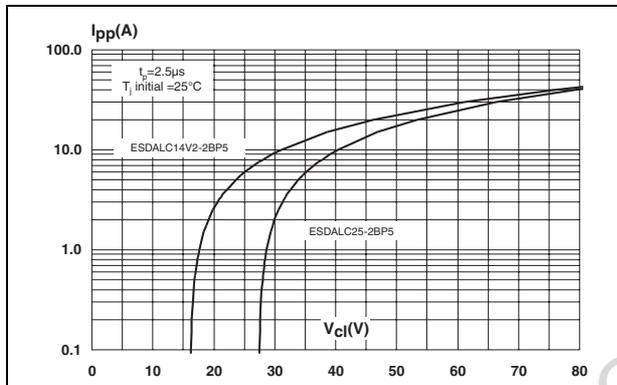


Figure 4. Junction capacitance versus reverse applied voltage (typical values)

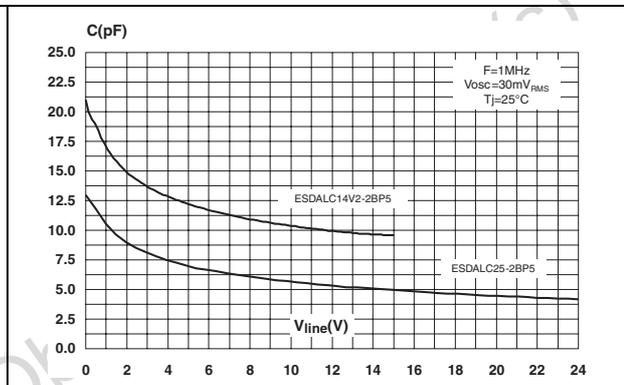


Figure 5. Relative variation of leakage current versus junction temperature (typical values)

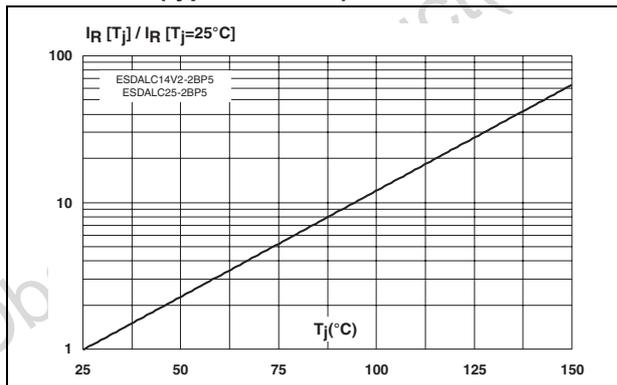
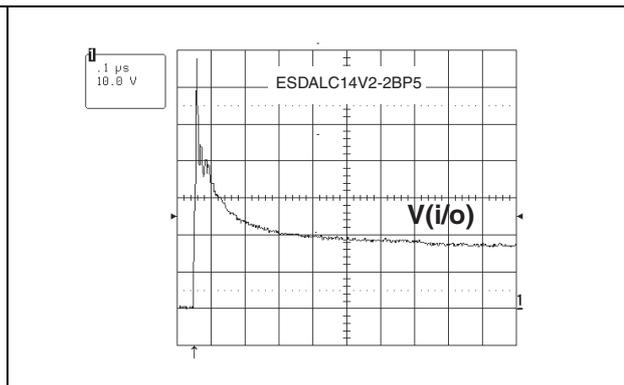
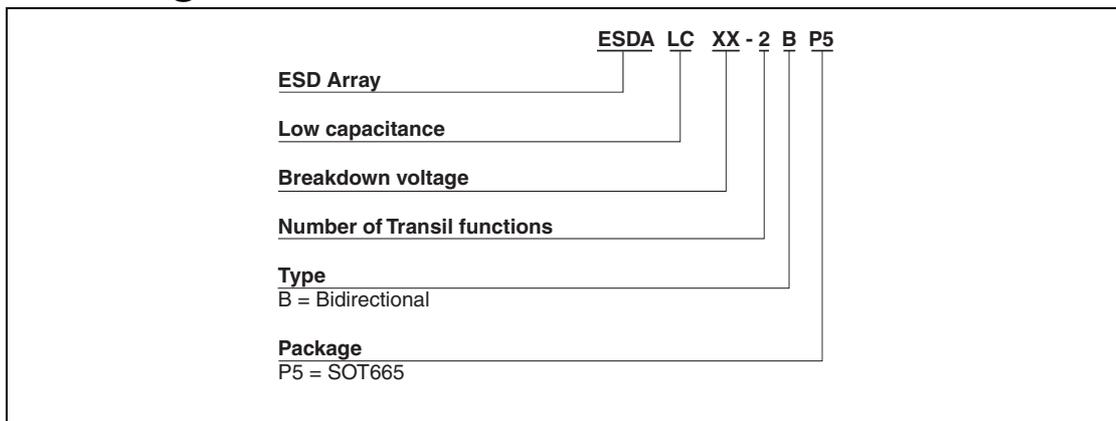


Figure 6. ESD response to IEC61000-4-2 (air discharge 15kV, positive surge)



2 Ordering information scheme

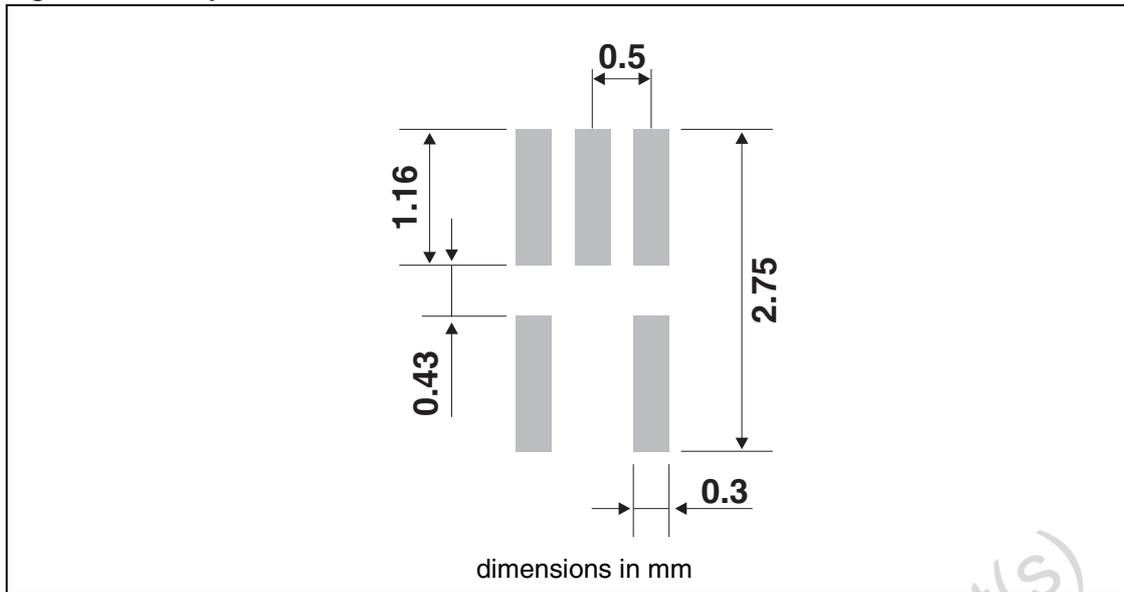


3 Package mechanical data

3.1 SOT665 package

| REF. | DIMENSIONS | | | |
|------|-------------|------|--------|-------|
| | Millimeters | | Inches | |
| | Min. | Max. | Min. | Max. |
| A | 0.50 | 0.60 | 0.020 | 0.024 |
| bp | 0.17 | 0.27 | 0.007 | 0.011 |
| c | 0.08 | 0.18 | 0.003 | 0.007 |
| D | 1.50 | 1.70 | 0.060 | 0.067 |
| E | 1.10 | 1.30 | 0.043 | 0.051 |
| e | 1.00 | | 0.040 | |
| e1 | 0.50 | | 0.020 | |
| He | 1.50 | 1.70 | 0.059 | 0.067 |
| Lp | 0.10 | 0.30 | 0.004 | 0.012 |

Figure 7. Footprint dimensions



In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

4 Ordering information

| Part Number | Marking | Package | Weight | Base qty | Delivery mode |
|-----------------|---------|---------|--------|----------|---------------|
| ESDALC14V2-2BP5 | A3 | SOT665 | 2.9 mg | 3000 | Tape & reel |
| ESDALC25-2BP5 | A4 | | | | |

5 Revision history

| Date | Revision | Changes |
|-------------|----------|-------------|
| 08-Dec-2005 | 1 | First issue |

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