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Vishay Siliconix

Automotive N-Channel 40 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	40				
$R_{DS(on)}(\Omega)$ at $V_{GS} = 10 \text{ V}$	0.0017				
$R_{DS(on)}(\Omega)$ at $V_{GS} = 4.5 \text{ V}$	0.0020				
I _D (A)	200				
Configuration	Single				
Package	TO-263-7L				

FEATURES

• TrenchFET® power MOSFET

N-Channel MOSFET

- Package with low thermal resistance
- 100 % R_q and UIS tested
- AEC-Q101 qualified d
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>





ABSOLUTE MAXIMUM RATIN	45 (16 = 25 °C; arriess		,		
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		V_{DS}	40	V	
Gate-Source Voltage	V_{GS}	± 20	V		
Continuous Drain Current	T _C = 25 °C ^a	l _D	200		
	T _C = 125 °C		193		
Continuous Source Current (Diode Condu	ction) ^a	I _S	200	Α	
Pulsed Drain Current b		I _{DM}	600		
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	95		
Single Pulse Avalanche Energy	L = U.1 MH	E _{AS}	451	mJ	
M · B Bi · i ii b	T _C = 25 °C	D	375	W	
Maximum Power Dissipation ^b	T _C = 125 °C	P_{D}	125		
Operating Junction and Storage Temperature Range		T _J , T _{sta}	-55 to +175	°C	

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	LIMIT	UNIT	
Junction-to-Ambient	PCB Mount ^c	R_{thJA}	40	°C/W	
Junction-to-Case (Drain)		R_{thJC}	0.4	G/VV	

Notes

- a. Package limited.
- b. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %.
- c. When mounted on 1" square PCB (FR4 material).
- d. Parametric verification ongoing.



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PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static				l		I.	
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		40	-	-	V
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} =	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$		2.0	2.5	V
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA
		V _{GS} = 0 V	V _{DS} = 40 V	-	-	1	
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V	V _{DS} = 40 V, T _J = 125 °C	-	-	50	μΑ
		V _{GS} = 0 V	V _{DS} = 40 V, T _J = 175 °C	-	-	250	1
On-State Drain Current ^a	I _{D(on)}	V _{GS} = 10 V	$V_{DS} \ge 5 \text{ V}$	200	-	=.	Α
		V _{GS} = 10 V	I _D = 30 A	-	0.0012	0.0017	
Drain-Source On-State Resistance a	В	V _{GS} = 10 V	I _D = 30 A, T _J = 125 °C	-	-	0.0028	Ω
Drain-Source On-State Resistance a	R _{DS(on)}	V _{GS} = 10 V	I _D = 30 A, T _J = 175 °C	-	-	0.0034	
		V _{GS} = 4.5 V	I _D = 20 A	-	0.0014	0.0020	
Forward Transconductance b	9fs	V _{DS} = 15 V, I _D = 30 A		-	181	-	S
Dynamic ^b							
Input Capacitance	C _{iss}			-	8934	11 168	pF
Output Capacitance	Coss	$V_{GS} = 0 V$	$V_{DS} = 20 \text{ V}, f = 1 \text{ MHz}$	-	1592	1990	
Reverse Transfer Capacitance	C _{rss}			-	928	1160	
Total Gate Charge ^c	Q_g			-	194	291	
Gate-Source Charge ^c	Q_{gs}	V _{GS} = 10 V	$V_{DS} = 20 \text{ V}, I_D = 20 \text{ A}$	-	25	-	nC
Gate-Drain Charge ^c	Q_{gd}			-	40	-	
Gate Resistance	R_g	f = 1 MHz		0.25	0.8	1.8	Ω
Turn-On Delay Time ^c	t _{d(on)}	$V_{DD} = 20 \text{ V, } R_L = 1 \Omega$ $I_D \cong 20 \text{ A, } V_{GEN} = 10 \text{ V, } R_g = 1 \Omega$		-	22	33	- ns
Rise Time ^c	t _r			-	17	26	
Turn-Off Delay Time ^c	t _{d(off)}			-	70	105	
Fall Time ^c	t _f			-	16	24	
Source-Drain Diode Ratings and Chara	cteristics ^b						
Pulsed Current ^a	I _{SM}			-	-	600	Α
Forward Voltage	V_{SD}	I _F = 60 A, V _{GS} = 0 V		_	0.8	1.5	V

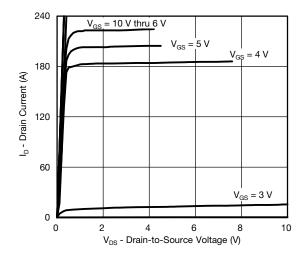
Notes

- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

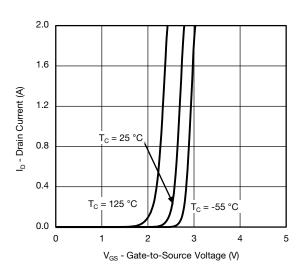
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



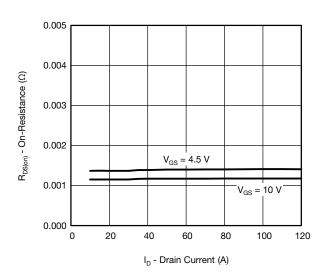
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



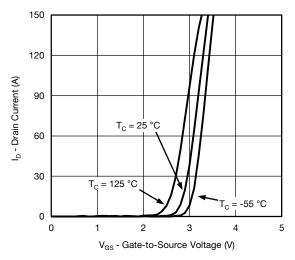
Output Characteristics



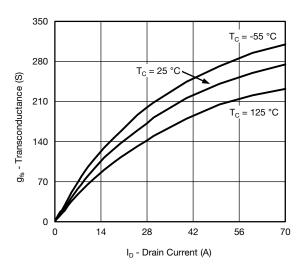
Transfer Characteristics



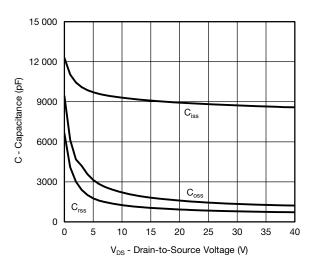
On-Resistance vs. Drain Current



Transfer Characteristics



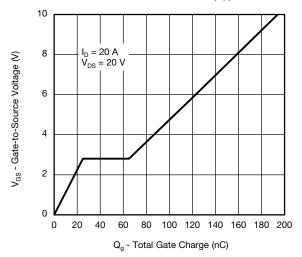
Transconductance



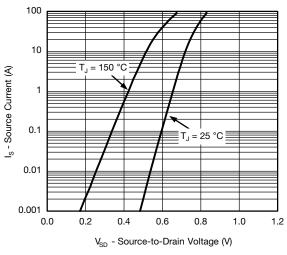
Capacitance



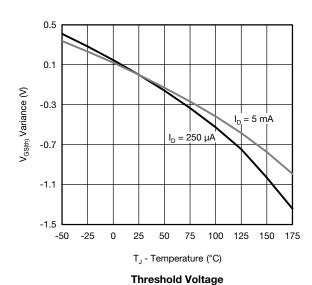
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)

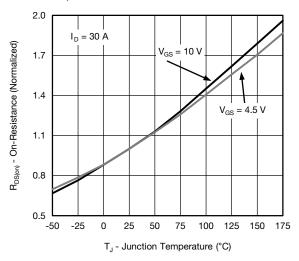


Gate Charge

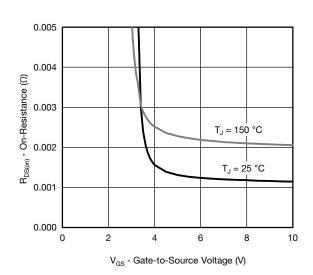


Source Drain Diode Forward Voltage

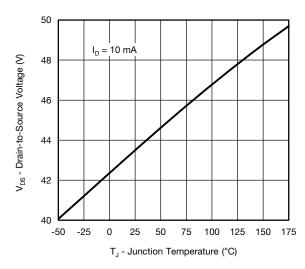




On-Resistance vs. Junction Temperature



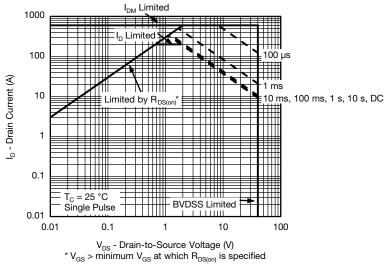
On-Resistance vs. Gate-to-Source Voltage



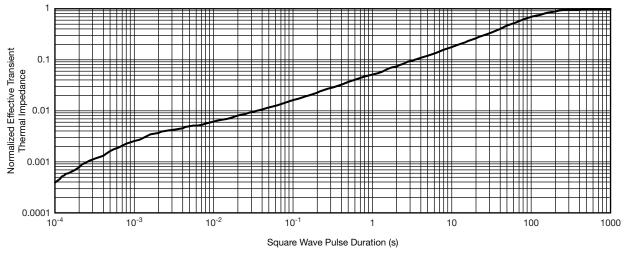
Drain Source Breakdown vs. Junction Temperature



THERMAL RATINGS ($T_A = 25$ °C, unless otherwise noted)



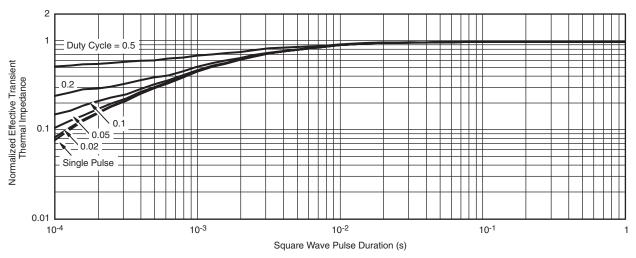
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

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THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
 - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?67058.



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REVISION	HISTORY a	
REVISION	DATE	DESCRIPTION OF CHANGE
В	04-Aug-15	Revised R _g minimum limit

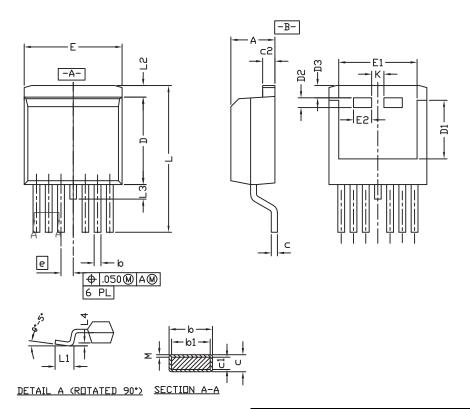
Note

a. As of April 2014





D²PAK (TO-263-7L) Case Outline



Notes

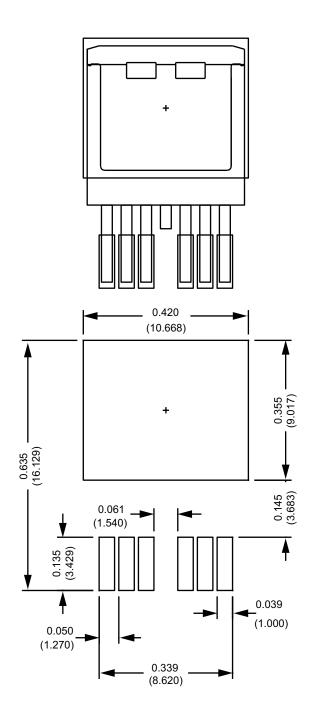
- 1. Plane B includes maximum features of heat sink tab and plastic
- 2. No more than 25 % of L1 can fall above seating plane by max. 8 mils
- 3. Pin to pin coplanarity max. 4 mils
- 4. Lead thickness 25 mils
- 5. For SUM part numbers lead thickness is 24 mils to 29 mils
- 6. For reference only
- 7. Use inches as the primary measurement
- 8. This feature is only for SUM

	INCHES		MILLIMETERS		
DIM.	MIN.	MAX.	MIN.	MAX.	
Α	0.160	0.190	4.064	4.826	
b	0.020	0.039	0.508	0.990	
b1	0.020	0.035	0.508	0.889	
c* SUB	0.012	0.018	0.305	0.457	
c* SUM	0.022	0.028	0.559	0.711	
c1	0.018	0.025	0.457	0.635	
c2	0.045	0.055	1.143	1.397	
D	0.340	0.380	8.636	9.652	
D1	0.260	0.280	6.604	7.112	
D2	0.046	0.050	1.168	1.270	
D3	0.045	0.055	1.143	1.397	
E	0.380	0.410	9.652	10.414	
E1	0.245	-	6.223	-	
E2	0.072	0.078	1.829	1.981	
е	0.050	BSC	1.27 BSC		
K	0.045	0.055	1.143	1.397	
L	0.575	0.625	14.605	15.875	
L1	0.090	0.110	2.286	2.794	
L2	0.040	0.055	1.016	1.397	
L3	0.050	0.070	1.270	1.778	
L4	0.010 BSC		0.254 BSC		
М	-	0.002	-	0.050	
ECN: T22-0410-Rev. D, 19-Sep-2022 DWG: 6006					

Revision: 19-Sep-2022 Document Number: 63782



Recommended Land Pattern D²PAK (TO-263-7L)





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