



N-Channel 100 V (D-S) MOSFET

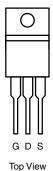
PRODUCT SUMMARY					
V _{DS} (V)	$R_{DS(on)}\left(\Omega\right)Max.$	I _D (A)	Q _g (Typ.)		
	0.021 at V _{GS} = 10 V	50 ^d			
100	0.023 at V _{GS} = 8 V	49.7	30.2 nC		
	0.028 at V _{GS} = 6 V	45			

FEATURES

- TrenchFET® Power MOSFET
- 100 % R_q and UIS Tested
- Material categorization: For definitions of compliance please see www.vishav.com/doc?99912



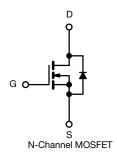
TO-220AB



Ordering Information: SUP50N10-21P-GE3 (Lead (Pb)-free and Halogen-free)

APPLICATIONS

- DC/AC Inverters
- Primary Side Switching
- Synchronous Rectification



ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)					
Parameter	Symbol	Limit	Unit		
Drain-Source Voltage	V _{DS}	100	V		
Gate-Source Voltage	V _{GS}	± 20	─		
Continuous Drain Current (T _{.1} = 150 °C)	T _C = 25 °C	1-	50 ^d		
Continuous Diam Current (1j = 130 °C)	T _C = 70 °C	I _D	41.6	A	
Pulsed Drain Current (t = 300 μs)	I _{DM}	60	7		
Avalanche Current	I _{AS}	40			
Single Avalanche Energy ^a L = 0.1 mH		E _{AS}	80	mJ	
Mariana Barra Biraina in al	T _C = 25 °C	В	125 ^b	10/	
Maximum Power Dissipation ^a	T _A = 25 °C ^c	$ P_D$ $-$	3.1	W	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Limit	Unit		
Junction-to-Ambient (PCB Mount) ^c	R _{thJA}	40	°C/W		
Junction-to-Case (Drain)	R _{thJC}	1	C/VV		

Notes:

- a. Duty cycle \leq 1 %.
- b. See SOA curve for voltage derating.
- c. When mounted on 1" square PCB (FR-4 material).
- d. Package limited.

SUP50N10-21P

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SPECIFICATIONS (T _J = 25)	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static	1 -7				1		
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	100		.,,		
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2	4	4	V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 250	nA	
		V _{DS} = 100 V, V _{GS} = 0 V			1		
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 100 V, V _{GS} = 0 V, T _J = 125 °C			50	μΑ	
		V _{DS} = 100 V, V _{GS} = 0 V, T _J = 150 °C			250		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 10 \text{ V}, V_{GS} = 10 \text{ V}$	20			Α	
		V _{GS} = 10 V, I _D = 10 A		0.017	0.021	Ω	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 8 V, I _D = 9.6 A		0.019	0.023		
		$V_{GS} = 6 \text{ V}, I_D = 8.7 \text{ A}$		0.022	0.028		
Forward Transconductance ^a	9 _{fs}	V _{DS} = 20 V, I _D = 10 A		40		S	
Dynamic ^b	•						
Input Capacitance	C _{iss}			2055			
Output Capacitance	C _{oss}	$V_{GS} = 0 \text{ V}, V_{DS} = 50 \text{ V}, f = 1 \text{ MHz}$		227		pF	
Reverse Transfer Capacitance	C _{rss}			120			
Total Gate Charge ^c	Q_g			45	68		
Gate-Source Charge ^c	Q _{gs}	$V_{DS} = 50 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 10 \text{ A}$		10.5		nC	
Gate-Drain Charge ^c	Q_{gd}			15.9			
Gate Resistance	R_g	f = 1 MHz	0.3	1.5	3	Ω	
Turn-On Delay Time ^c	t _{d(on)}			10	20		
Rise Time ^c	t _r	$V_{DD} = 20 \text{ V}, R_L = 2 \Omega$		10	20	ns	
Turn-Off Delay Time ^c	t _{d(off)}	$I_D \cong 8 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		22	33		
Fall Time ^c	t _f			7	14		
Drain-Source Body Diode Ratings ar	nd Characteri	stics (T _C = 25 °C) ^b					
Continuous Current	I _S				50	۸	
Pulsed Current	I _{SM}	1			60	Α	
Forward Voltage ^a	V_{SD}	I _F = 8 A, V _{GS} = 0 V		0.75	1.2	٧	
Reverse Recovery Time	t _{rr}			55	83	ns	
Peak Reverse Recovery Current	I _{RM(REC)}	I _F = 8 A, dI/dt = 100 A/μs		4.1	6.2	Α	
Reverse Recovery Charge	Q _{rr}			107	161	nC	

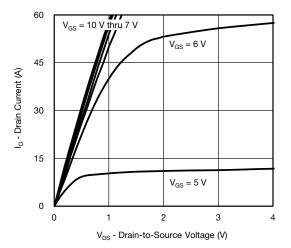
Notes:

- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

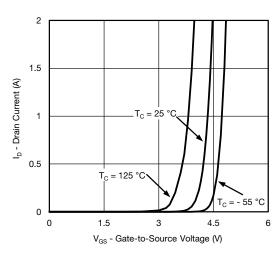
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



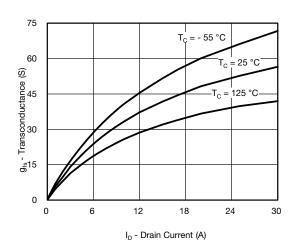
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



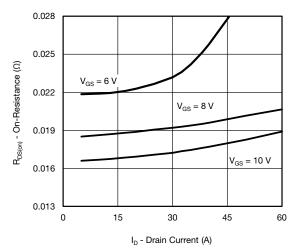
Output Characteristics



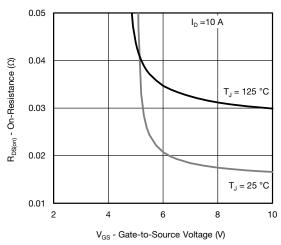
Transfer Characteristics



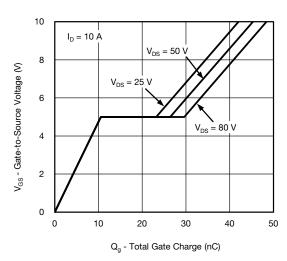
Transconductance



On-Resistance vs. Drain Current



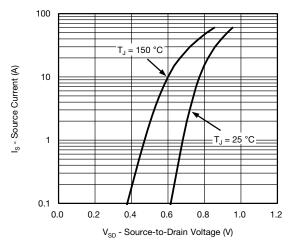
On-Resistance vs. Gate-to-Source Voltage



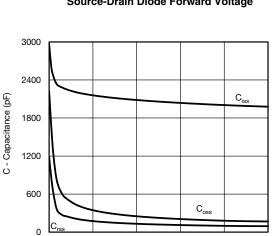
Gate Charge

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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

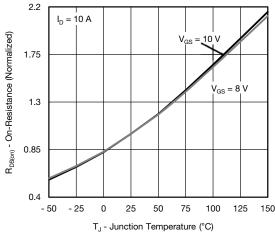


Source-Drain Diode Forward Voltage

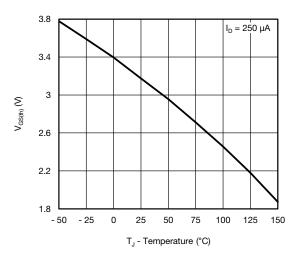


V_{DS} - Drain-to-Source Voltage (V) Capacitance

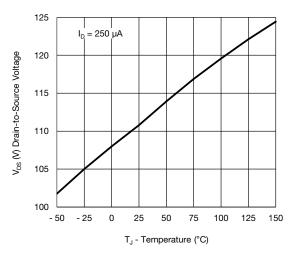
100



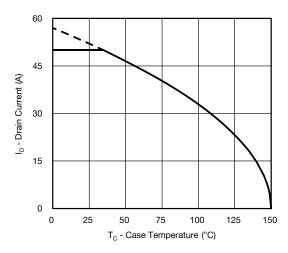
On-Resistance vs. Junction Temperature



Threshold Voltage



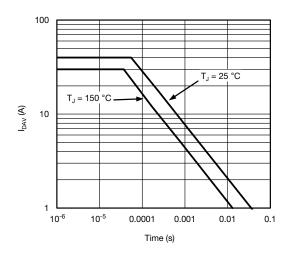
Drain Source Breakdown vs. Junction Temperature

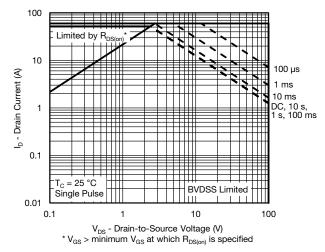


Current Derating



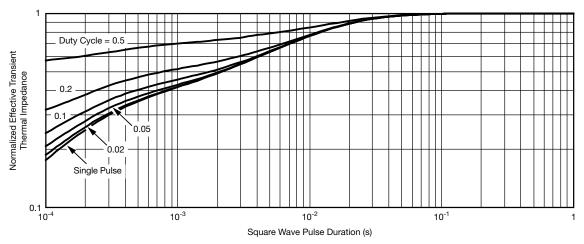
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)





Single Pulse Avalanche Current Capability vs. Time





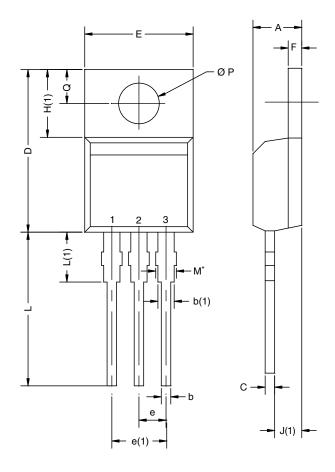
Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62781.





TO-220AB



	D2

	MILLIMETERS		INC	HES	
DIM.	MIN.	MAX.	MIN.	MAX.	
А	4.25	4.65	0.167	0.183	
b	0.69	1.01	0.027	0.040	
b(1)	1.20	1.73	0.047	0.068	
С	0.36	0.61	0.014	0.024	
D	14.85	15.49	0.585	0.610	
D2	12.19	12.70	0.480	0.500	
Е	10.04	10.51	0.395	0.414	
е	2.41	2.67	0.095	0.105	
e(1)	4.88	5.28	0.192	0.208	
F	1.14	1.40	0.045	0.055	
H(1)	6.09	6.48	0.240	0.255	
J(1)	2.41	2.92	0.095	0.115	
L	13.35	14.02	0.526	0.552	
L(1)	3.32	3.82	0.131	0.150	
ØΡ	3.54	3.94	0.139	0.155	
Q	2.60	3.00	0.102	0.118	
ECN: T14-0413-Rev. P, 16-Jun-14 DWG: 5471					

Note

 $^{^{\}star}$ M = 1.32 mm to 1.62 mm (dimension including protrusion) Heatsink hole for HVM



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