W-LAN+Bluetooth Combo Module Data Sheet

Cypress Chipset CYW54591
for 802.11a/b/g/n/ac 2x2 MIMO, RSDB
+ Bluetooth 5.2

Tentative P/N : LBEE5XV1XA-TEMP

This Datasheet is preliminary version, and subject to change without notice.

Revision History

Revision Code	Date	Description	Comments
-	Apr. 18 2019	First Issue	
A	Jun. 5 2020	9. MODULE PIN DESCRIPTIONS	Changed the name of pin 57 from VDDIO_SD to VDDIO. Changed the name of pin 31 from RF_SW_CTRL13 to RF_SW_CTRL11.
B	Jul. 17 2020	8. DIMENSIONS	Added Solder bump and defined T1 dimension
C	Oct. 29 2020	2. KEY FEATURE 4. SAMPLE ORDERING INFORMATION 6. OPERATING CONDITION 11. I/O States 14. ELECTORICAL CHARACTERISTICS	Added Weight information. Changed sample and EVB P/N. Added operating temperature spec. Corrected Typ. VBAT from 3.6V to 3.3V Added I/O State Table Added Output power spec.
D	Nov. 11 2020	8. DIMENSIONS, MARKING AND TERMINAL CONFIGURATIONS 10. REFERENCE PERIPHERAL CIRCUIT	Added Marking information. Added Reference circuit.
E	Dec. 14 2020	1. SCOPE 14.9. DC/RF Characteristics for Bluetooth	Modified Bluetooth version. Corrected Minimum output power.
F	Jan. 28 2021	8. DIMENSIONS, MARKING AND TERMINAL CONFIGURATIONS 14. ELECTORICAL CHARACTERISTICS	Added pin 1 mark information on Bottom view. Added current consumption information.
G	Feb. 1 2021	14.7. DC/RF Characteristics for IEEE802.11ac(HT 40MHz) - 5GHz 14.8. DC/RF Characteristics for IEEE802.11ac(HT 80MHz) - 5GHz	Optimized the max value of current consumption for VHT40/80 of 5GHz mode.

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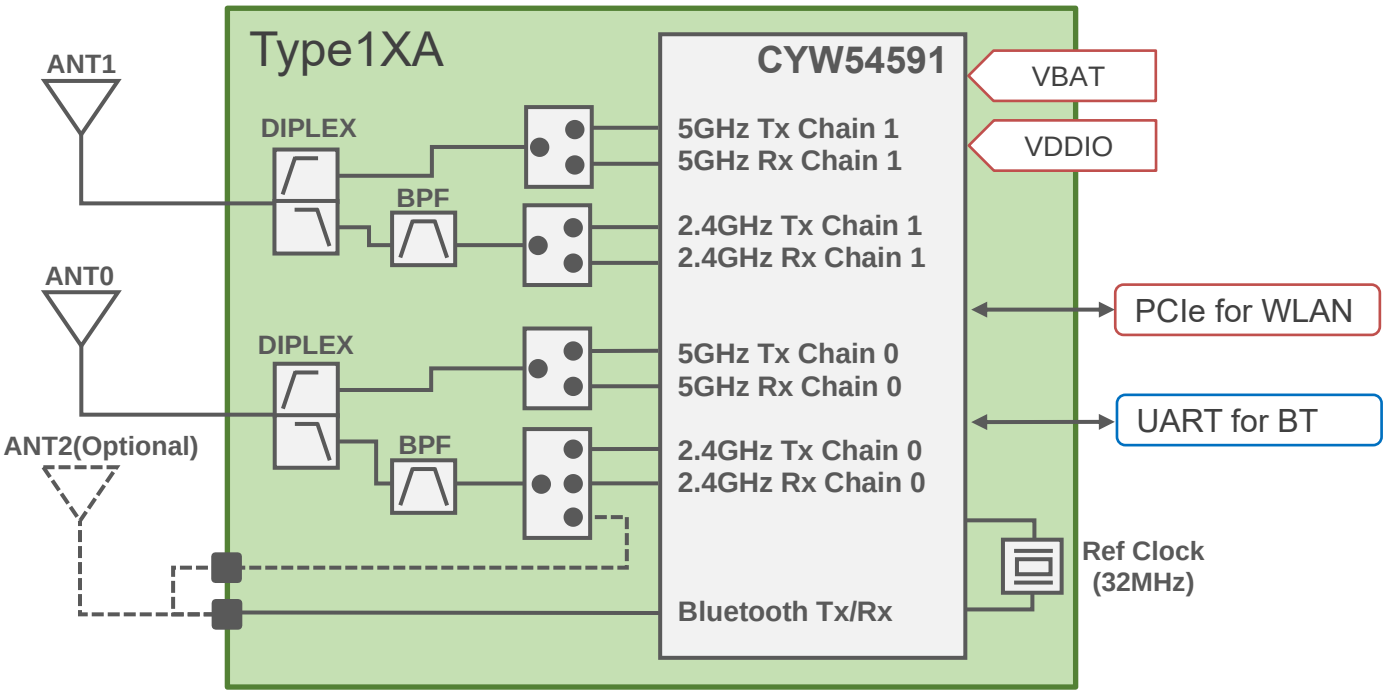
1. SCOPE

This specification is applied to the IEEE802.11a/b/g/n/ac W-LAN 2x2 MIMO + Bluetooth 5.2 combo module.

2. KEY FEATURE

- Cypress CYW54591 inside
- Compliant with IEEE802.11a/b/g/n/ac, 5G MIMO, RSDB (Real Simultaneous Dual Band)
- Compliant with Bluetooth specification v5.2
- Supports standard PCIe Interface for WLAN
- Interface support for Bluetooth is Host Controller Interface (HCI)
- Surface mount type 11.4 x 8.9 mm(Typical), H = 1.4 mm(Max.)
- Weight : 0.36g
- MSL : 3
- RoHS compliant

3. BLOCK DIAGRAM



4. SAMPLE ORDERING INFORMATION

Ordering Part Number	Description
LBEE5XV1XA-SMP	In case of sample order
LBEE5XV1XA-EVB	Evaluation Board

5. ABSOLUTE MAXIMUM RATINGS

Parameter		Min	Max	Unit
Storage Temperature		-40	+85	deg.C
Supply Voltage	VBAT	-0.5	+6.0	V
	VDDIO	-0.5	+3.9	V

Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability. No damage assuming only one parameter is set at limit at a time with all other parameters is set within operating condition.

6. OPERATING CONDITION

Parameter		Min	Typ	max	Unit
Operating Temperature		-40	25	85	deg.C
Operating Voltage	VBAT	3.0	3.3	4.8	V
	VDDIO	1.62	1.8 or 3.3	3.63	V

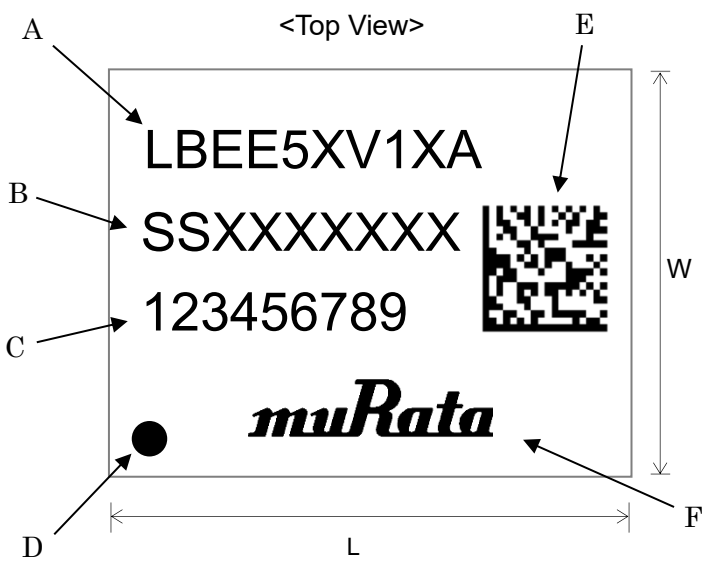
Note) Min. voltage of VBAT is sensitive to get RF performance, so please keep min. voltages level at the input of these module terminals, otherwise RF performance significantly goes worse.

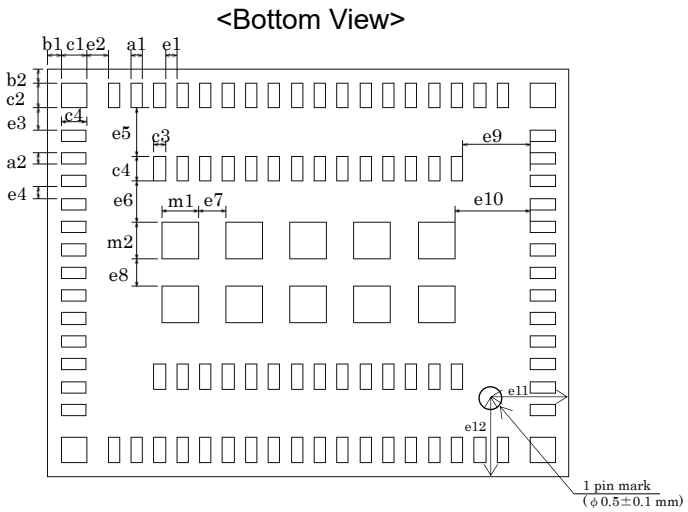
7. EXTERNAL LPO_IN SIGNAL REQUIREMENT

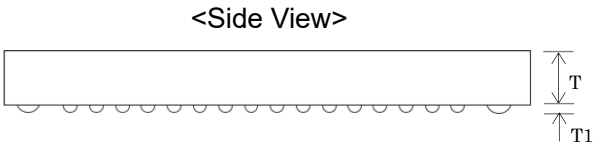
Parameter	External LPO_IN Clock	Unit
Nominal input frequency	32.768	kHz
Frequency accuracy	+/-250	ppm
Duty cycle	30-70	%
Input signal amplitude	200 - 3300	mV, p-p
Signal type	Square-wave or sine-wave	-
Input impedance[1]	> 100k	ohm
	< 5	pF
Clock jitter (during initial start-up)	<10,000	ppm

[1] When power is applied or switch off.

8. DIMENSIONS, MARKING AND TERMINAL CONFIGURATIONS







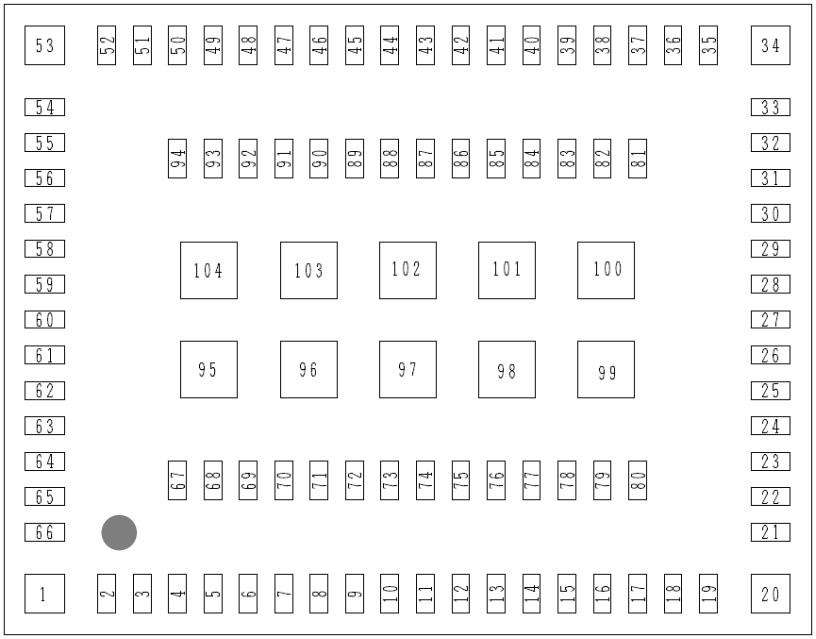
Marking	Meaning
A	Module Part Number
B	Inspection Number
C	Serial Number
D	Pin 1 Marking
E	2D code
F	Murata Logo

Mark	Dimensions	Mark	Dimensions	Mark	Dimensions	Mark	Dimensions
L	11.4 ± 0.2	W	8.9 ± 0.2	T	1.4 max.	T1	0.04 typ.
a1	0.25 ± 0.1	a2	0.25 ± 0.1	b1	0.3 ± 0.2	b2	0.3 ± 0.2
c1	0.55 ± 0.1	c2	0.55 ± 0.1	c3	0.25 ± 0.1	c4	0.55 ± 0.1
e1	0.25 ± 0.1	e2	0.475 ± 0.1	e3	0.475 ± 0.1	e4	0.25 ± 0.1
e5	1.05 ± 0.1	e6	0.9 ± 0.1	e7	0.6 ± 0.1	e8	0.6 ± 0.1
e9	1.475 ± 0.1	e10	1.65 ± 0.1	e11	1.787 ± 0.2	e12	1.609 ± 0.2
m1	0.8 ± 0.1	m2	0.8 ± 0.1				

(unit : mm)

9. MODULE PIN DESCRIPTIONS

<TOP VIEW>



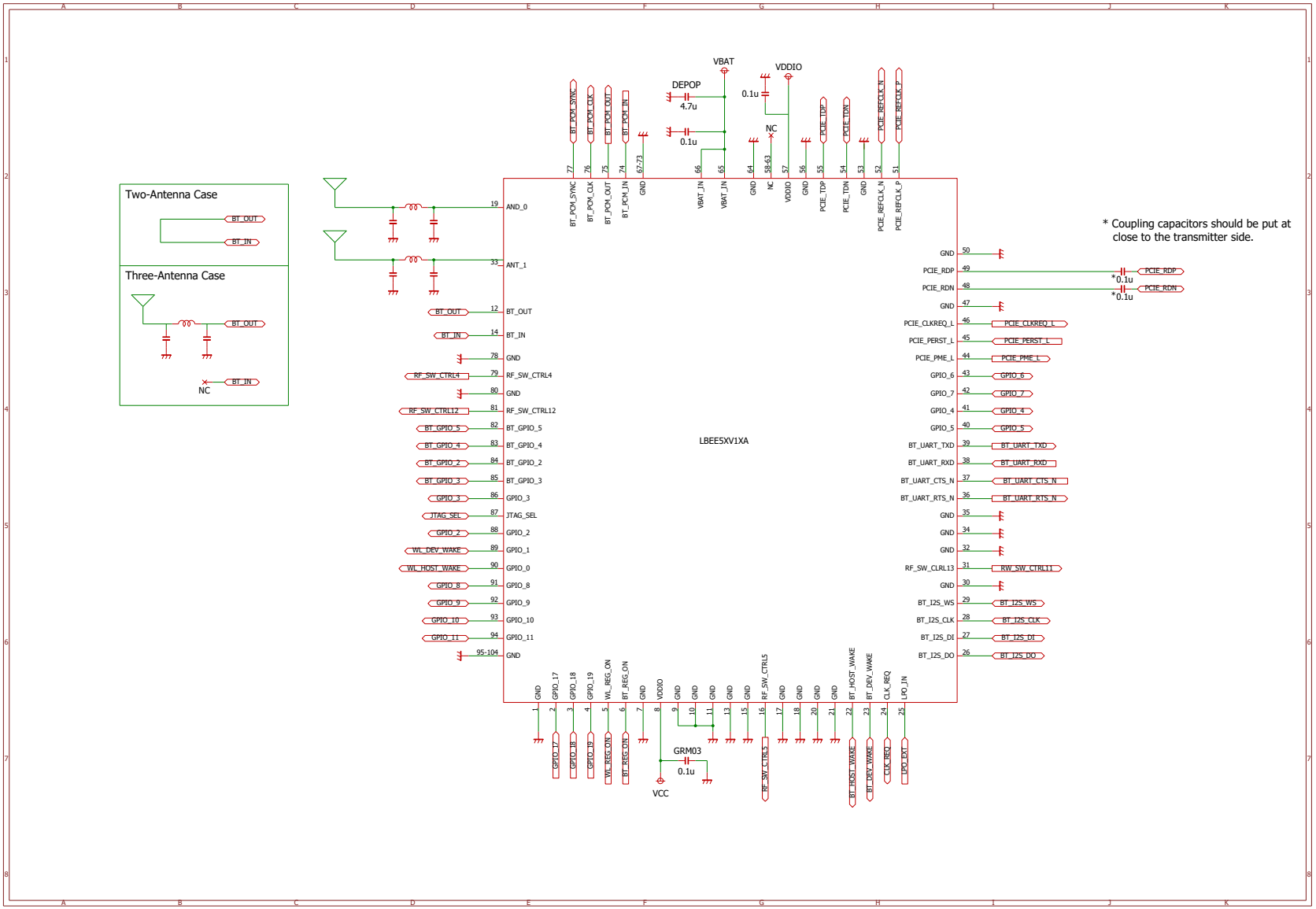
No.	Terminal Name	No.	Terminal Name	No.	Terminal Name
1	GND	31	RF_SW_CTRL11	61	NC
2	GPIO_17	32	GND	62	NC
3	GPIO_18	33	ANT_1	63	NC
4	GPIO_19	34	GND	64	GND
5	WL_REG_ON	35	GND	65	VBAT
6	BT_REG_ON	36	BT_UART_RTS_N	66	VBAT
7	GND	37	BT_UART_CTS_N	67-73	GND
8	VDDIO	38	BT_UART_RXD	74	BT_PCM_IN
9	GND	39	BT_UART_TXD	75	BT_PCM_OUT
10	GND	40	GPIO_5	76	BT_PCM_CLK
11	GND	41	GPIO_4	77	BT_PCM_SYNC
12	BT_OUT	42	GPIO_7	78	GND
13	GND	43	GPIO_6	79	RF_SW_CTRL4
14	BT_IN	44	PCIE_PME_L	80	GND
15	GND	45	PCIE_PERST_L	81	RF_SW_CTRL12
16	RF_SW_CTRL5	46	PCIE_CLKREQ_L	82	BT_GPIO_5
17	GND	47	GND	83	BT_GPIO_4
18	GND	48	PCIE_RDN	84	BT_GPIO_2
19	ANT_0	49	PCIE_RDP	85	BT_GPIO_3
20	GND	50	GND	86	GPIO_3
21	GND	51	PCIE_REFCLKP	87	JTAG_SEL
22	BT_HOST_WAKE	52	PCIE_REFCLKN	88	GPIO_2
23	BT_DEV_WAKE	53	GND	89	GPIO_1
24	CLK_REQ	54	PCIE_TDN	90	GPIO_0
25	LPO_IN	55	PCIE_TDP	91	GPIO_8
26	BT_I2S_DO	56	GND	92	GPIO_9
27	BT_I2S_DI	57	VDDIO	93	GPIO_10
28	BT_I2S_CLK	58	NC	94	GPIO_11
29	BT_I2S_WS	59	NC	95-104	GND
30	GND	60	NC		

No.	Pin name	Type	Connection to IC pin name	Description
1	GND	-	-	Ground
2	GPIO_17	I/O	GPIO_17	Programmable GPIO Pin
3	GPIO_18	I/O	GPIO_18	Programmable GPIO Pin
4	GPIO_19	I/O	GPIO_19	Programmable GPIO Pin
5	WL_REG_ON	I	WL_REG_ON	Used by PMU to power up or power down the internal CYW54591 regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. This pin has an internal 200k ohm pull-down resistor that is enabled by default. It can be disabled through programming.
6	BT_REG_ON	I	BT_REG_ON	Used by PMU to power up or power down the internal CYW54591 regulators used by the Bluetooth section. Also, when deasserted, this pin holds the Bluetooth section in reset. This pin has an internal 200k ohm pull-down resistor that is enabled by default. It can be disabled through programming.
7	GND	-	-	Ground
8	VDDIO	I	SYS_VDDIO WCC_VDDIO BT_VDDO VDDIO	IO supply
9	GND	-	-	Ground
10	GND	-	-	Ground
11	GND	-	-	Ground
12	BT_OUT			
13	GND	-	-	Ground
14	BT_IN			
15	GND	-	-	Ground
16	RF_SW_CTRL5	O	O	Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.
17	GND	-	-	Ground
18	GND	-	-	Ground
19	ANT_0	-	-	RF Port for WLAN (2.4GHz & 5GHz) and BT
20	GND	-	-	Ground
21	GND	-	-	Ground
22	BT_HOST_WAKE	O	BT_HOST_WAKE	Host wake-up: Signal from the module to the host indicating that the module requires attention.
23	BT_DEV_WAKE	I	BT_DEV_WAKE	Bluetooth device wake-up: Signal from the host to the module indicating that the host requires attention.
24	CLK_REQ	I/O	CLK_REQ	Reference clock request (shared by BT and WLAN). If not used, this can be no-connect.
25	LPO_IN	I	LPO_IN	External sleep clock input (32.768 kHz)
26	BT_I2S_DO	I/O	BT_I2S_DO	I^2S data output
27	BT_I2S_DI	I/O	BT_I2S_DI	I^2S data input
28	BT_I2S_CLK	I/O	BT_I2S_CLK	I^2S clock, can be master (output) or slave (input).
29	BT_I2S_WS	I/O	BT_I2S_WS	I^2S WS, can be master (output) or slave (input).
30	GND	-	-	Ground
31	RF_SW_CTRL11	O	RF_SW_CTRL11	Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.

32	GND	-	-	Ground
33	ANT_1			RF Port for WLAN (2.4GHz & 5GHz)
34	GND	-	-	Ground
35	GND	-	-	Ground
36	BT_UART_RTS_N	O	BT_UART_RTS_N	UART request-to-send. Active-low request-to-send signal for the HCI UART interface. BT LED control pin.
37	BT_UART_CTS_N	I	BT_UART_CTS_N	UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface.
38	BT_UART_RXD	I	BT_UART_RXD	UART serial input. Serial data input for the HCI UART interface.
39	BT_UART_TXD	O	BT_UART_TXD	UART serial output. Serial data output for the HCI UART interface.
40	GPIO_5		GPIO_5	Programmable GPIO pins.
41	GPIO_4		GPIO_4	
42	GPIO_7		GPIO_7	
43	GPIO_6		GPIO_6	
44	PCIE_PME_L	OD	PCIE_PME_L	PCI power management event output. Used to request a change in the device
45	PCIE_PERST_L	I	PCIE_PERST_L	PCIe System Reset. This input is the PCIe reset as defined in the PCIe base specification version 1.1. PCIE_PERST_L pad excludes internal pull-up.
46	PCIE_CLKREQ_L	OD	PCIE_CLKREQ_L	PCIe clock request signal which indicates when the REFCLK to the PCIe interface can be gated. 1 = the clock can be gated. 0 = the clock is required.
47	GND	-	-	Ground
48	PCIE_RDN	I	PCIE_RDN0	Receiver differential pair (x1 lane).
49	PCIE_RDP	I	PCIE_RDP0	Receiver differential pair (x1 lane).
50	GND	-	-	Ground
51	PCIE_REFCLKP	I	PCIE_REFCLKP	PCIE Differential Clock inputs (negative and positive). 100 MHz differential.
52	PCIE_REFCLKN	I	PCIE_REFCLKN	
53	GND	-	-	Ground
54	PCIE_TDN	O	PCIE_TDN0	Transmitter differential pair (×1 lane).
55	PCIE_TDP	O	PCIE_TDP0	
56	GND	-	-	Ground
57	VDDIO	I	VDDIO	IO supply
58	NC	-	-	No Connect
59	NC	-	-	No Connect
60	NC	-	-	No Connect
61	NC	-	-	No Connect
62	NC	-	-	No Connect
63	NC	-	-	No Connect
64	GND	-	-	Ground
65	VBAT		SR_VDDBAT5V LDO_VDDBAT5V	VBAT supply
66				
67-73	GND	-	-	Ground
74	BT_PCM_IN	I	BT_PCM_IN	PCM data input.

75	BT_PCM_OUT	O	BT_PCM_OUT	PCM data output.
76	BT_PCM_CLK	I/O	BT_PCM_CLK	PCM clock; can be master (output) or slave (input).
77	BT_PCM_SYNC	I/O	BT_PCM_SYNC	PCM sync; can be master (output) or slave (input).
78	GND	-	-	Ground
79	RF_SW_CTRL4	O	RF_SW_CTRL4	Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.
80	GND	-	-	Ground
81	RF_SW_CTRL12	O	RF_SW_CTRL12	Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.
82	BT_GPIO_5	I/O	BT_GPIO_5	Bluetooth general-purpose I/O.
83	BT_GPIO_4	I/O	BT_GPIO_4	
84	BT_GPIO_2	I/O	BT_GPIO_2	
85	BT_GPIO_3	I/O	BT_GPIO_3	
86	GPIO_3	I/O	GPIO_3	Programmable GPIO pins.
87	JTAG_SEL	I/O	JTAG_SEL	JTAG select: pull high to select the JTAG interface. If the JTAG interface is not used this pin may be left floating or connected to ground.
88	GPIO_2	I/O	GPIO_2	Programmable GPIO pins.
89	GPIO_1	I/O	GPIO_1	
90	GPIO_0	I/O	GPIO_0	
91	GPIO_8	I/O	GPIO_8	
92	GPIO_9	I/O	GPIO_9	
93	GPIO_10	I/O	GPIO_10	
94	GPIO_11	I/O	GPIO_11	
95-104	GND	-	-	Ground

10. REFERENCE PERIPHERAL CIRCUIT



11. I/O States

The following notations are used in I/O State Table.

- I: Input signal
- O: Output signal
- I/O: Input/Output signal
- PU = Pulled up
- PD = Pulled down
- NoPull = Neither pulled up nor pulled down
- Where applicable, the default value is shown in bold brackets (for example, [default value])

I/O State Table

Name	I/O	Keeper	Active Mode	Low Power State/Sleep (All Power Present)	Power-down (BT_REG_ON and WL_REG_ON Held Low)	Out-of-Reset; Before SW Download (BT_REG_ON High; WL_REG_ON High)	Power-down (WL_REG_ON High and BT_REG_ON=0) and VDDIOs Are Present	Power Rail
WL_REG_ON BT_REG_ON	I	N	I: PD Pull-down can be disabled	I: PD Pull-down can be disabled	I: PD (of 200K)	I: PD (of 200K)	I: PD (of 200K)	–
GPIO_0	I/O	Y	I/O: PU, PD, NoPull Programmable [PD]	I/O: PU, PD, NoPull Programmable [PD]	High-Z, NoPull	I: PD	I: PD	VDDIO
GPIO_1	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
GPIO_2	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPullb	I: NoPull	VDDIO
GPIO_3	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPullb	I: NoPull	VDDIO
GPIO_4	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPullb	I: NoPull	VDDIO
GPIO_5	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPullb	I: NoPull	VDDIO
GPIO_6	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPullb	I: NoPull	VDDIO
GPIO_7	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
GPIO_8	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
GPIO_9	I/O	Y	I/O: PU, PD, NoPull Programmable [PU]	I/O: PU, PD, NoPull Programmable [NoPull]	I: PU	I: PU	I:PU	VDDIO

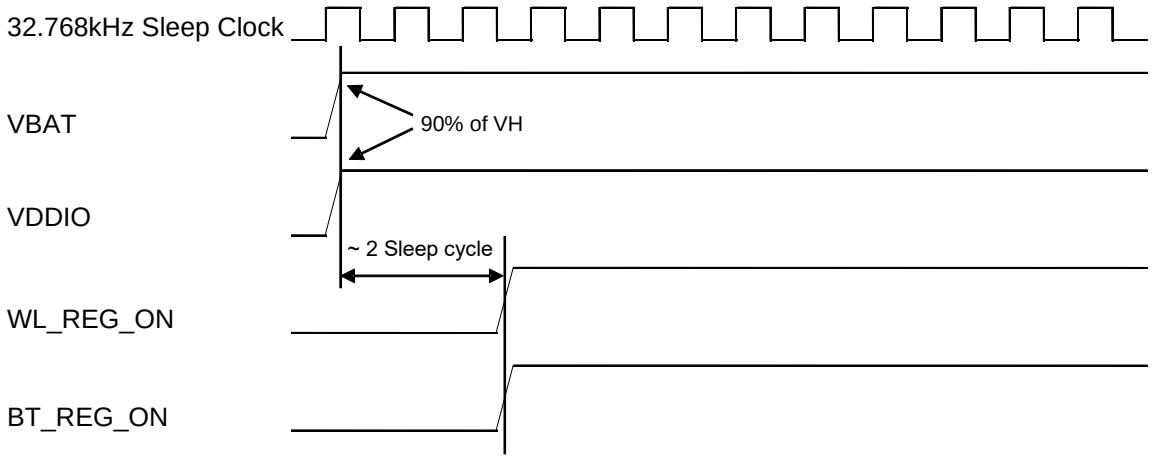
GPIO_10	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
GPIO_11	I/O	Y	I/O: PU, PD, NoPull Programmable [PU]	I/O: PU, PD, NoPull Programmable [PU]	I: PU	I: PU	I:PU	VDDIO
GPIO_17	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
GPIO_18	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
GPIO_19	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
RF_SW_CTRL_X	O	N	O: NoPull	O: NoPull	High-Z, NoPull	O: NoPull	O: NoPull	VDDIO_RF
CLK_REQ	O	Y	Open drain or push-pull (programmable).Active high.	Open drain or push-pull (programmable).Active high.	High-Z, NoPull	Open drain. Active high	Open drain. Active high	BT_VDDO
BT_HOST_WAKE	O	Y	Input/Output; PU, PD, NoPull (programmable)	Input/Output; PU, PD, NoPull (programmable)	High-Z, NoPull	Input, PU	Input, PD	BT_VDDO
BT_DEV_WAKE	I	Y	Input/Output; PU, PD, NoPull (programmable)	Input/Output; PU, PD, NoPull (programmable)	High-Z, NoPull	Input, PD	Input, PD	BT_VDDO
BT_GPIO_2 BT_GPIO_3	I/O	Y	Input/Output; PU, PD, NoPull (programmable)	Input/Output; PU, PD, NoPull (programmable)	High-Z, NoPull	Input, PD	Input, PD	BT_VDDO
BT_GPIO_4 BT_GPIO_5	I/O	Y	Input/Output; PU, PD, NoPull (programmable)	Input/Output; PU, PD, NoPull (programmable)	High-Z, NoPull	Input, PU	Input, PU	BT_VDDO
BT_UART_CTS_N	I	Y	Input, NoPull	Input, NoPull	High-Z, NoPull	Input, PU	Input, PU	BT_VDDO
BT_UART_RTS_N	O	Y	Output, NoPull	Output, NoPull	High-Z, NoPull	Input, PU	Input, PU	BT_VDDO
BT_UART_RXD	I	Y	Input, NoPull	Input, NoPull	High-Z, NoPull	Input, PU	Input, PU	BT_VDDO
BT_UART_TXD	O	Y	Output, NoPull	Output, NoPull	High-Z, NoPull	Input, PU	Input, PU	BT_VDDO
BT_PCM_CLK	I/O	Y	Input, NoPull	Input, NoPull	High-Z, NoPull	Input, PD	Input, PD	BT_VDDO
BT_PCM_IN	I/O	Y	Input, NoPull	Input, NoPull	High-Z, NoPull	Input, PD	Input, PD	BT_VDDO
BT_PCM_OUT	I/O	Y	Input, NoPull	Input, NoPull	High-Z, NoPull	Input, PD	Input, PD	BT_VDDO
BT_PCM_SYNC	I/O	Y	Input, NoPull	Input, NoPull	High-Z, NoPull	Input, PD	Input, PD	BT_VDDO
BT_I^2S_CLK	I/O	Y	Input, NoPull	Input, NoPull	High-Z, NoPull	High-Z, NoPull	High-Z, NoPull	BT_VDDO
BT_I^2S_DO	I/O	Y	Output, NoPull	Output, NoPull	High-Z, NoPull	Input, PD	Input, PD	BT_VDDO
BT_I^2S_DI	I/O	Y	Input, NoPull	Input, NoPull	High-Z, NoPull	Input, PD	Input, PD	BT_VDDO
BT_I^2S_WS	I/O	Y	Input, NoPull	Input, NoPull	High-Z, NoPull	High-Z, NoPull	High-Z, NoPull	BT_VDDO

12. POWER SEQUENCE

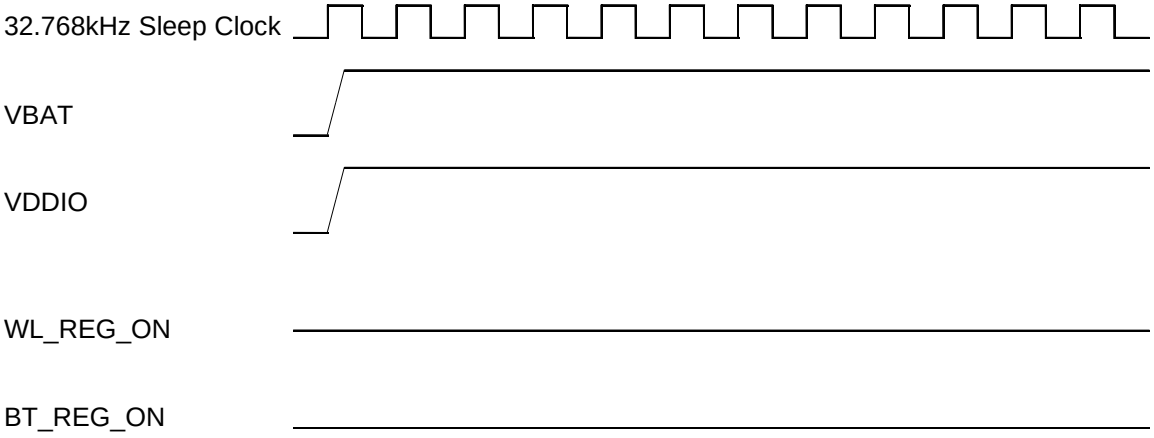
12.1. POWER ON SEQUENCE

- VBAT and VDDIO should not rise 10%-90% faster than 40 microseconds.
- VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present fast or be held high before VBAT is high.
- WL_REG_ON and BT_REG_ON should be up after sleep clock oscillation is stabilized.
- Please proceed reset by WL_REG_ON and BT_REG_ON until it starts normally if it doesn't wake from sleep property or it is presented with uncertain status.
- Please keep repeats power off sequence and power on sequence several times until it started normally.
- The CYW54591 has an internal Power-on reset (POR) circuit. The device will be held in reset for a maximum of 110 ms after internal regulators and VDDIO have passed the POR threshold. Wait at least 150 ms after WL_REG_ON is driven high before initiating PCIe accesses.

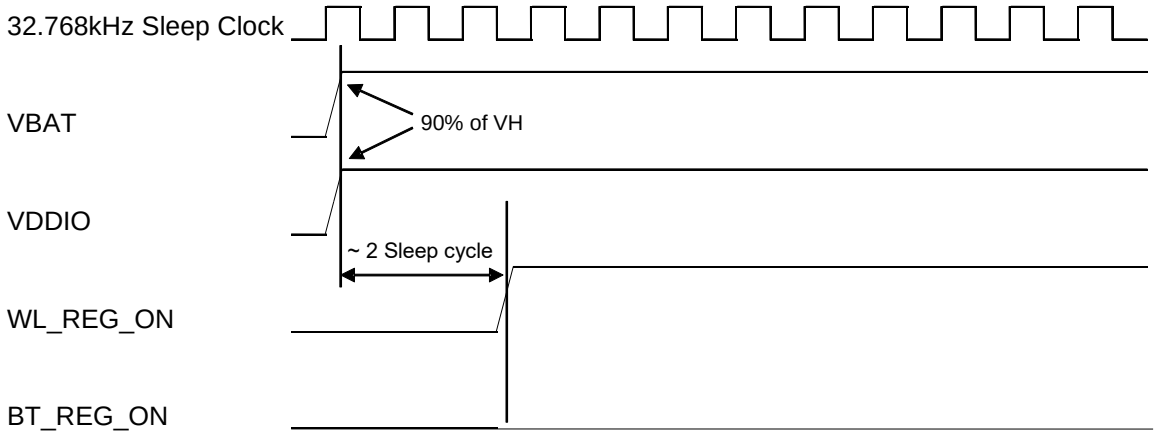
12.1.1. Power On Sequence for WLAN = ON and BT = ON



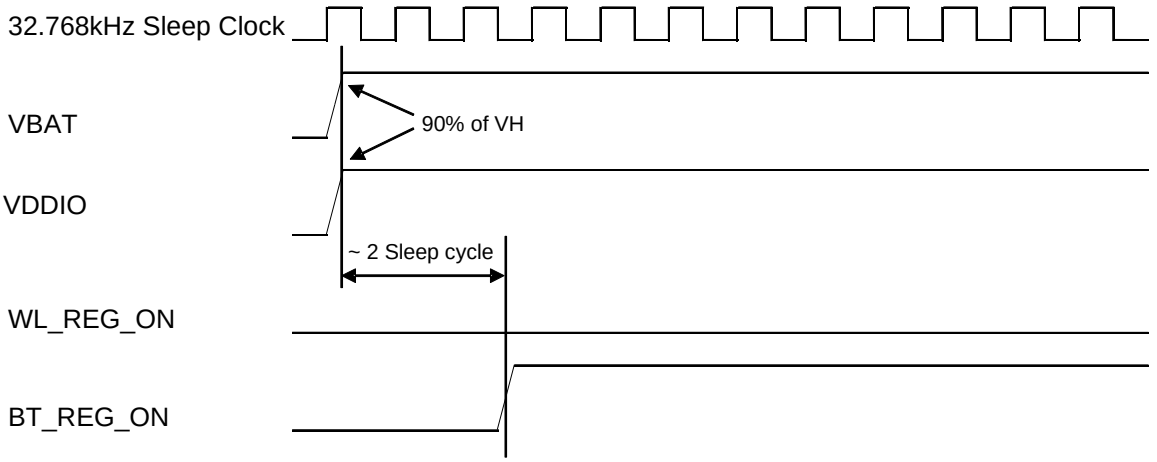
12.1.2. Power On Sequence for WLAN = OFF and BT = OFF



12.1.3. Power On Sequence for WLAN = ON and BT = OFF



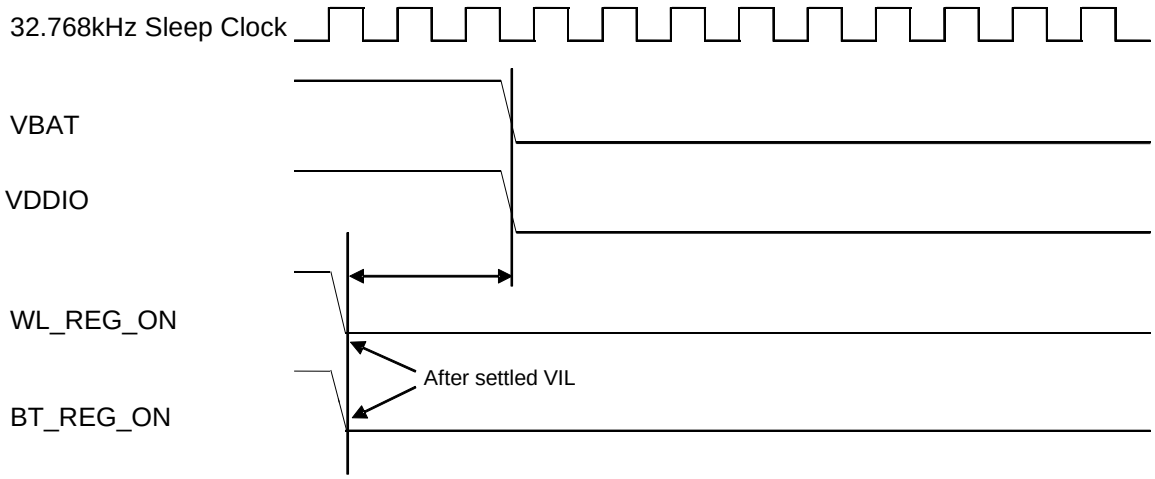
12.1.4. Power On Sequence for WLAN = OFF and BT = ON



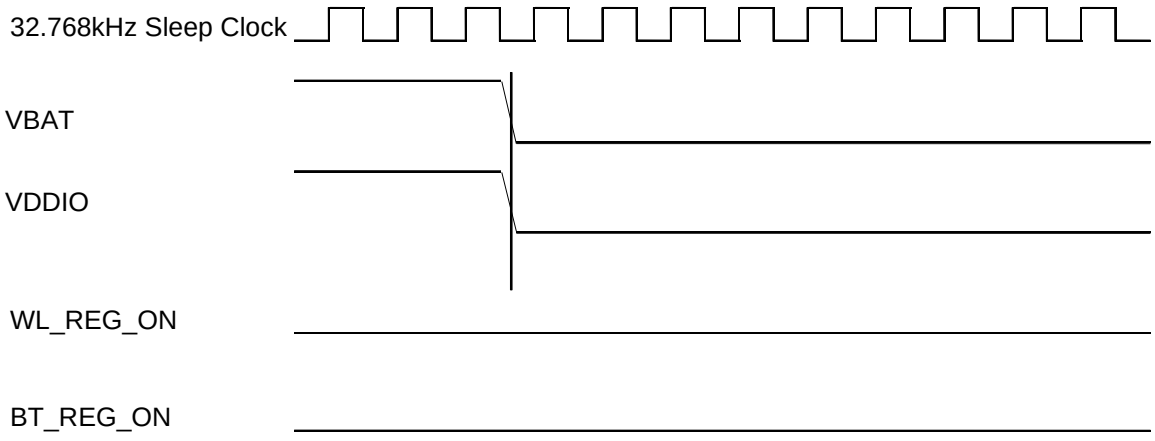
12.1.5. Power Off Sequence

- VDDIO should be down before or at the same time as VBAT. VBAT should NOT be down earlier than VDDIO low. VDDIO becomes low state is prior to VBAT low.
- VBAT and VDDIO should be down after WL_REG_ON and BT_REG_ON are low. Waiting time from REG_ON down to power supply off is not prescribed.

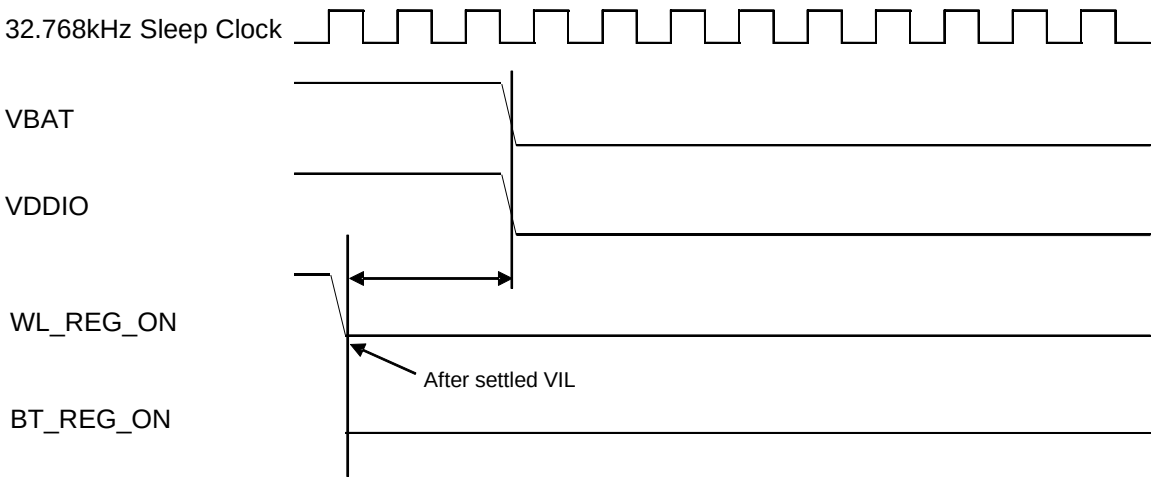
12.1.6. Power Off Sequence for WLAN = ON and BT = ON



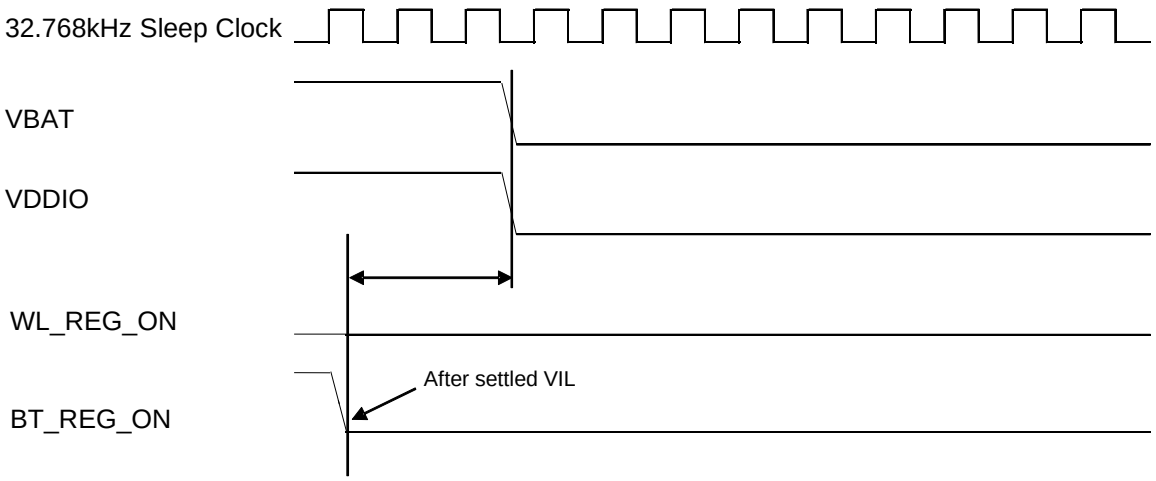
12.1.7. Power Off Sequence for WLAN = OFF and BT = OFF



12.1.8. Power Off Sequence for WLAN = ON and BT = OFF

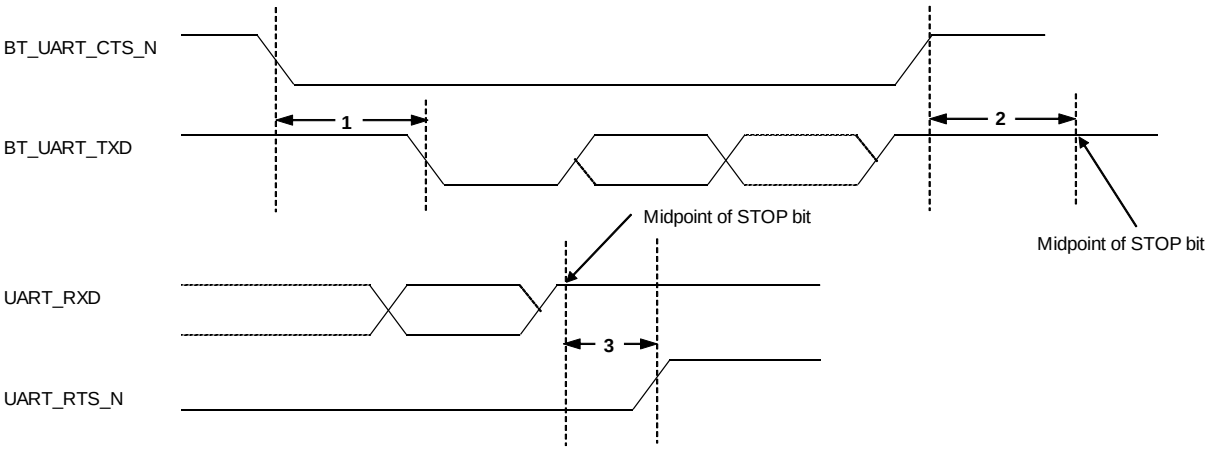


12.1.9. Power Off Sequence for WLAN = OFF and BT = ON



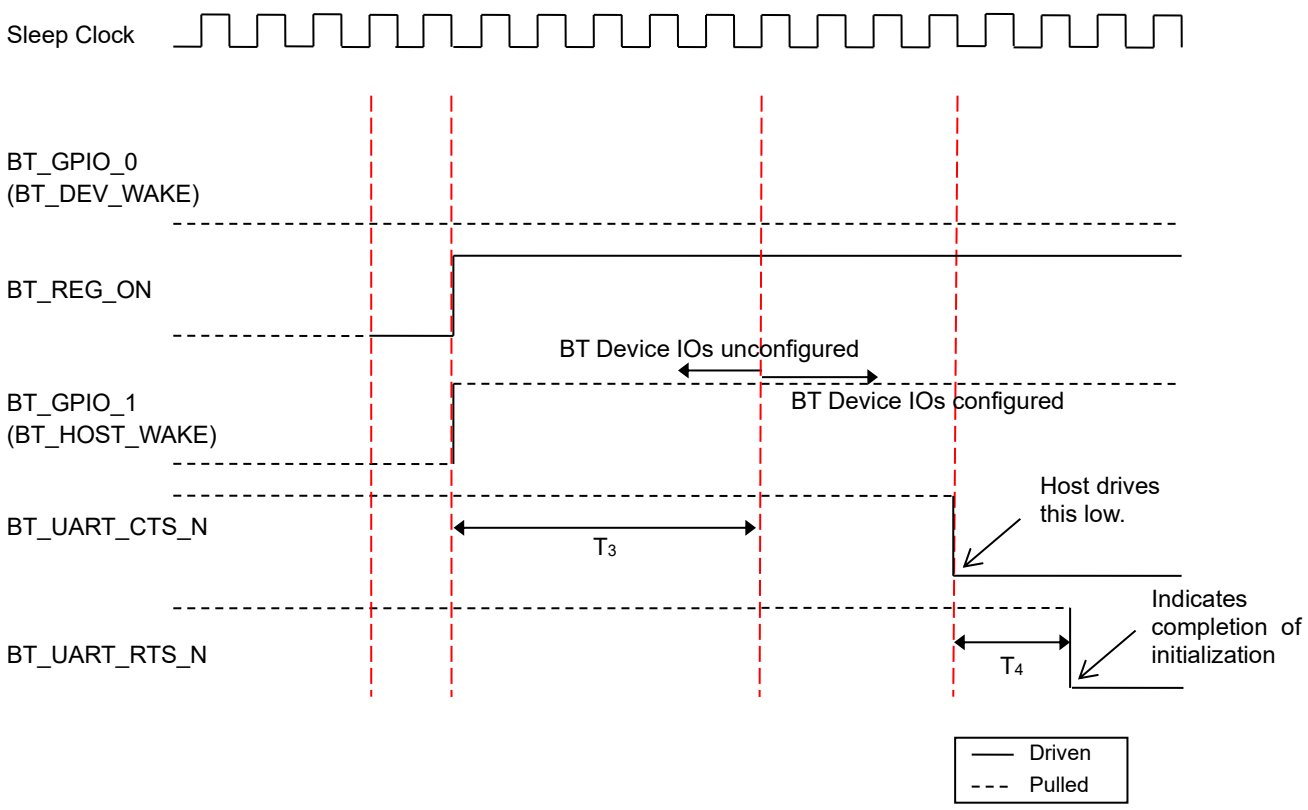
13. INTERFACE TIMING AND AC CHARACTERISTICS

13.1. Bluetooth UART Timing



Reference	Description	Min	Typ	Max	Unit
1	Delay time, UART_CTS_N low to UART_TXD valid	-	-	1.5	Bit periods
2	Setup time, UART_CTS_N high before midpoint of stop bit	-	-	0.5	Bit periods
3	Delay time, midpoint of stop bit to UART_RTS_N high	-	-	0.5	Bit periods

13.2. Bluetooth Startup Signaling Sequence



Reference	Description	Min	Typ	Max	Unit
T_3	Time for the BT device to settle its IOs after BT_REG_ON is asserted.	-	-	40.0	ms
T_4	Time for the BT device to drive UART_RTS_N low after the host drives UART_CTS_N low	-	-	10.0	ms

13.3. Bluetooth PCM Interface Timing

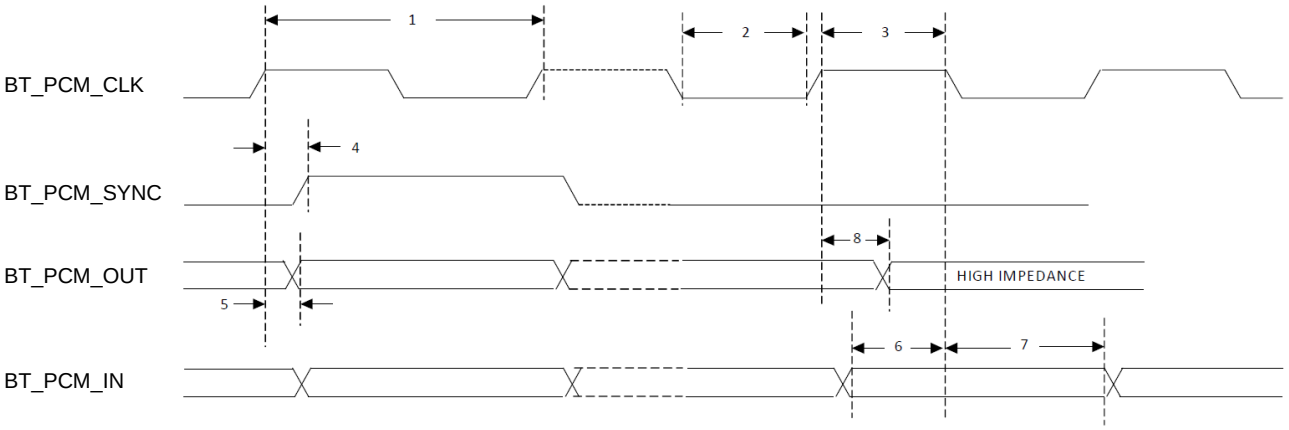
Data Formatting

The IC used in the module may be configured to generate and accept several different data formats. For conventional narrowband speech mode, the IC uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits can be configured to support various data formats on PCM interface. The remaining three bits are ignored on the input and may be filled with 0s, 1s, a sigh bit, or a programmed value on the output. The default format is 13bit 2's complement data, left justified, and clocked MSB first.

Wideband Speech Support

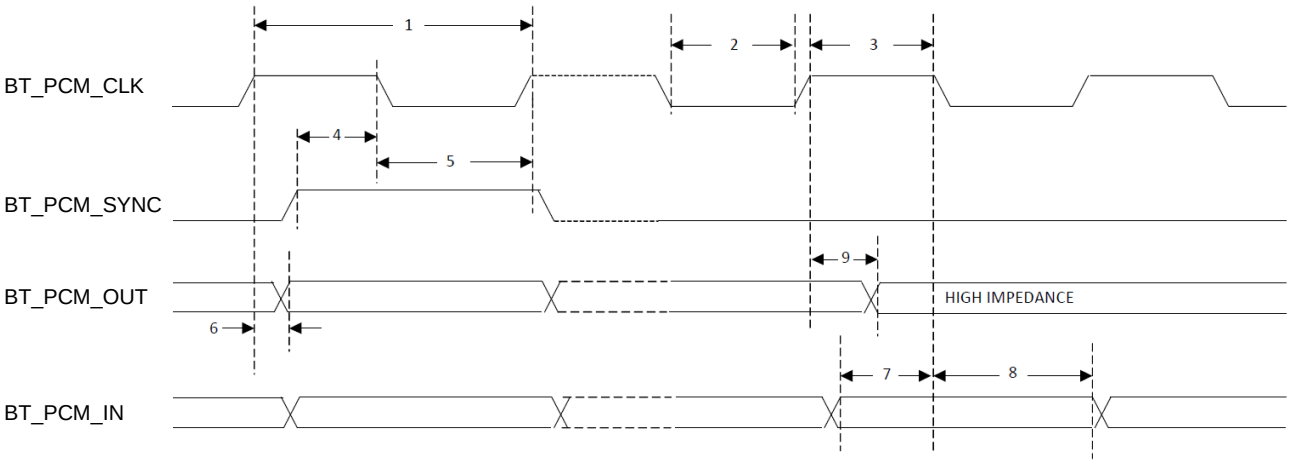
When the host encodes wideband speech (WBS) packets in transparent mode, the encoded packets are transferred over the PCM bus for an eSCO voice connection. In this mode, the PCM bus is typically configured in master mode for a 4kHz sync rate with 16-bit samples, resulting in a 64 kbps bit rate. The IC also supports slave transparent mode using a proprietary rate-matching scheme. IN SBC-code mode, linear 16-bit data at 16kHz (256kbps rate) is transferred over the PCM bus.

Short Frame Sync, Master Mode



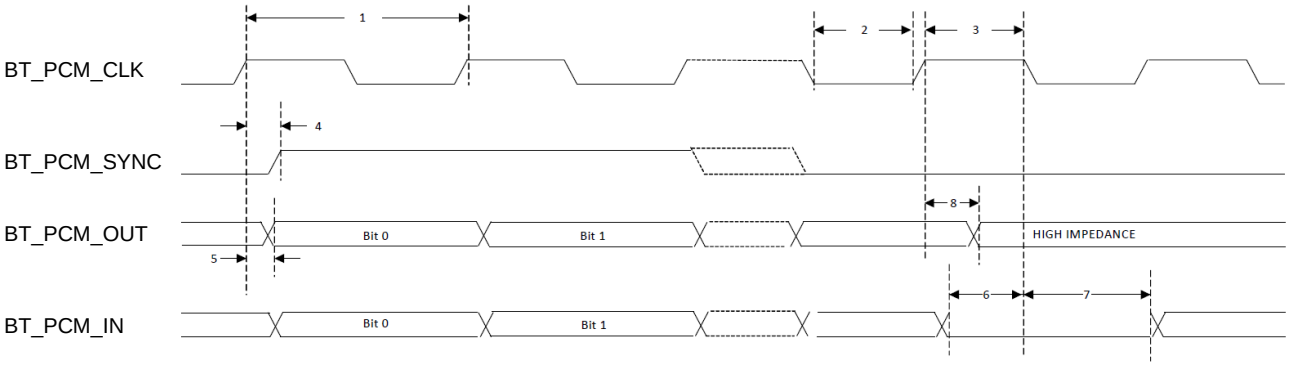
Reference	Description	Min	Typ	Max	Unit
1	PCM bit clock frequency	-	-	12.0	MHz
2	PCM bit clock High	41.0	-	-	ns
3	PCM bit clock Low	41.0	-	-	ns
4	PCM_SYNC delay	0	-	25.0	ns
5	PCM_OUT delay	0	-	25.0	ns
6	PCM_IN setup	8	-	-	ns
7	PCM_IN hold	8	-	-	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance.	0	-	25.0	ns

Short Frame Sync, Slave Mode



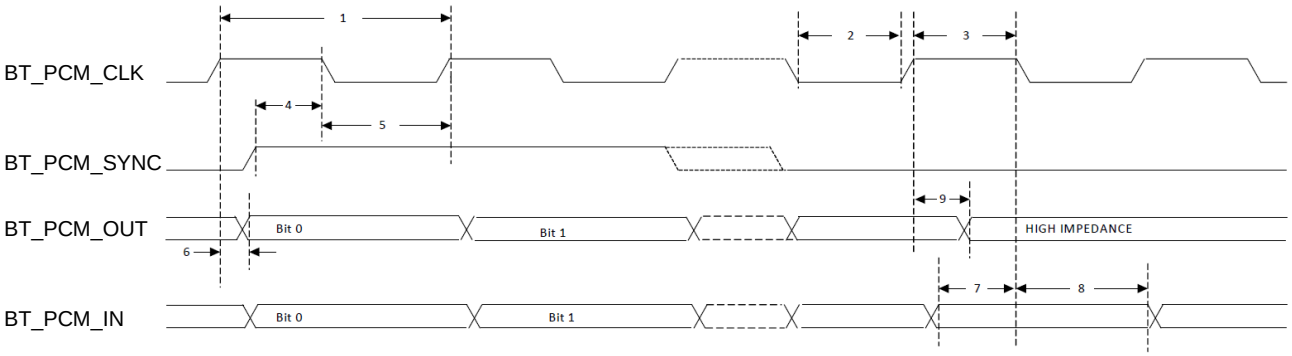
Reference	Description	Min	Typ	Max	Unit
1	PCM bit clock frequency	-	-	12.0	MHz
2	PCM bit clock High	41.0	-	-	ns
3	PCM bit clock Low	41.0	-	-	ns
4	PCM_SYNC setup	8.0	-	-	ns
5	PCM_SYNC hold	8.0	-	-	ns
6	PCM_OUT delay	0	-	25.0	ns
7	PCM_IN setup	8.0	-	-	ns
8	PCM_IN hold	8.0	-	-	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance.	0	-	25.0	ns

Long Frame Sync, Master Mode



Reference	Description	Min	Typ	Max	Unit
1	PCM bit clock frequency	-	-	12.0	MHz
2	PCM bit clock High	41.0	-	-	ns
3	PCM bit clock Low	41.0	-	-	ns
4	PCM_SYNC delay	0	-	25.0	ns
5	PCM_OUT delay	0	-	25.0	ns
6	PCM_IN setup	8.0	-	-	ns
7	PCM_IN hold	8.0	-	-	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	-	25.0	ns

Long Frame Sync, Slave Mode



Reference	Description	Min	Typ	Max	Unit
1	PCM bit clock frequency	-	-	12.0	MHz
2	PCM bit clock High	41.0	-	-	ns
3	PCM bit clock Low	41.0	-	-	ns
4	PCM_SYNC setup	8.0	-	-	ns
5	PCM_SYNC hold	8.0	-	-	ns
6	PCM_OUT delay	0	-	25.0	ns
7	PCM_IN setup	8.0	-	-	ns
8	PCM_IN hold	8.0	-	-	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance.	0	-	25.0	ns

13.4. Bluetooth I²S Interface Timing

The IC used in the module supports I²S format. The module supports only PCM digital audio ports through I²S format.
The I²S signals are:
- I²S clock: I²S SCK (Module pin: BT_PCM_CLK)
- I²S Word Select: I²S WS (Module pin: BT_PCM_SYNC)
- I²S Data Out: I²S SDO (Module pin: BT_PCM_OUT)
- I²S Data In: I²S SDI (Module pin: BT_PCM_IN)

I²S SCK and I²S WS become outputs in master mode and inputs in slave mode, while I²S SDO always stays as an output. The channel word length is 16 bits and the data is justified so that the MSB of the let-channel data is aligned with the MSB of the I²S bus, per the I²S specification. The MSB of each data word is transmitted one bit clock cycle after the I²S WS transition, synchronous with the falling edge of bit clock. Left-channel data is transmitted when I²S WS is low, and right-channel data is transmitted when I²S WS is high. Data bits sent by the CYW89335 are synchronized with the falling edge of I²S_SCK and should be sampled by the receiver on the rising edge of I²S_SCK.

The clock rate in master mode is either of the following:

48 kHz x 32 bits per frame = 1.536 MHz
48 kHz x 50 bits per frame = 2.400 MHz

The master clock is generated from the input reference clock using a N/M clock divider.

In the slave mode, any clock rate is supported to a maximum of 3.072 MHz.

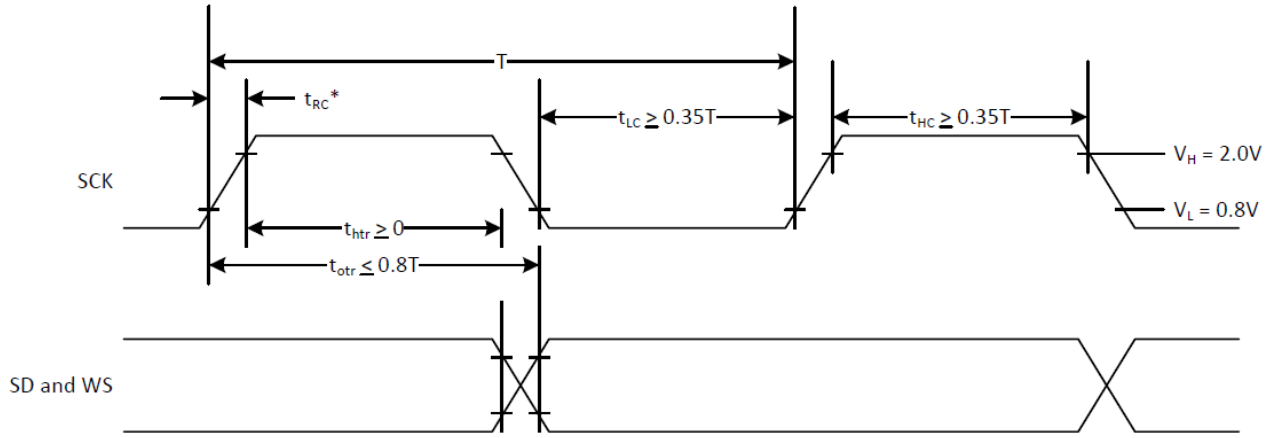
Timing for I²S Transmitters and Receivers

	Transmitter				Receiver				
	Lower Limit		Upper Limit		Lower Limit		Upper Limit		
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Notes
Clock Period T	T_{tr}	-	-	-	T_r	-	-	-	a
Master Mode: Clock generated by transmitter or receiver									
HIGH t_{HC}	$0.35T_{tr}$	-	-	-	$0.35T_{tr}$	-	-	-	b
LOW_{LC}	$0.35T_{tr}$	-	-	-	$0.35T_{tr}$	-	-	-	b
Slave Mode: Clock accepted by transmitter or receiver									
HIGH t_{HC}	-	$0.35T_{tr}$	-	-	-	$0.35T_{tr}$	-	-	c
LOW_{LC}	-	$0.35T_{tr}$	-	-	-	$0.35T_{tr}$	-	-	c
Rise time t_{RC}	-	-	$0.15T_{tr}$	-	-	-	-	-	d
Transmitter									
Delay t_{dtr}	-	-	-	0.8T	-	-	-	-	e
Hold time t_{htr}	0	-	-	-	-	-	-	-	d
Receiver									
Setup time t_{sr}	-	-	-	-	-	$0.2T_r$	-	-	f
Hold time t_{hr}	-	-	-	-	-	0	-	-	f

(a). The system clock period T must be greater than T_{tr} and T_r because both the transmitter and receiver have to be able to handle the data transfer rate.
(b). At all data rates in master mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason, t_{HC} and t_{LC} specified with respect to T.
(c). In slave mode, the transmitter and receiver need a clock signal with minimum HIGH and LOW periods so that they can detect the signal. So long as the minimum periods are greater than $0.35T_{tr}$ any clock that meets the requirements can be used.
(d). Because the delay(t_{dtr}) and the maximum transmitter speed (defined by T_{tr}) are related, a fast transmitter driven by a slow clock edge can result in t_{dtr} not exceeding t_{RC} which means t_{htr} becomes zero or negative. Therefore, the transmitter has guarantee that t_{htr} is greater than or equal to zero, so long as the clock rise-time t_{RC} is not more than t_{RC} where t_{RCmax} is not less than $0.15T_{tr}$.
(e). To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient setup time.
(f). The data setup and hold time must not be less than the specified receiver setup and hold time.

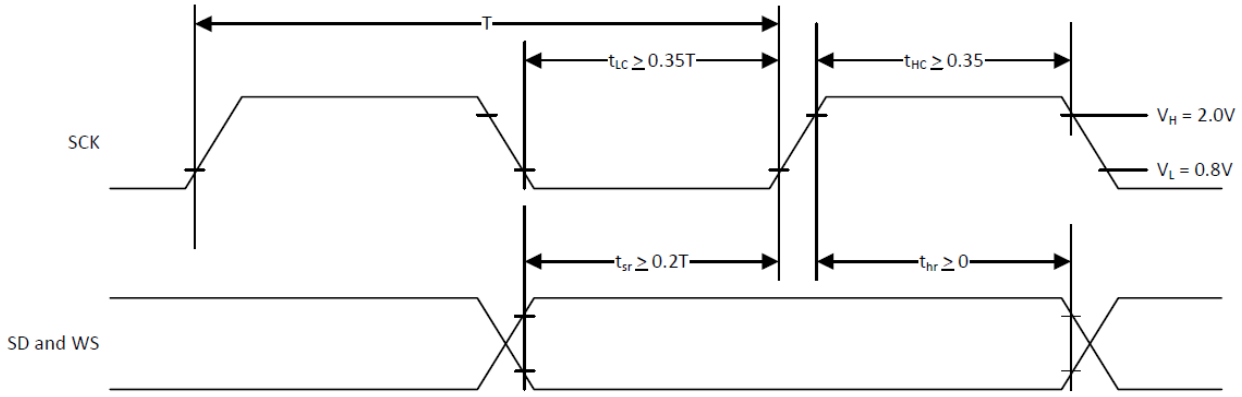
Note
The time periods specified in below figures are defined by the transmitter speed. The receiver specifications must match transmitter performance.

I²S Transmitters Timing



T = Clock period
T_{tr} = Minimum allowed clock period for transmitter
$T = T_{tr}$
* t_{RC} is only relevant for transmitters in slave mode.

I²S Receiver Timing



T = Clock period
T_r = Minimum allowed clock period for transmitter
$T > T_r$

14. ELECTORICAL CHARACTERISTICS

14.1. DC/RF Characteristics for IEEE802.11b - 2.4G

Normal Condition : 25deg.C, VBAT =3.3V.
11Mbps mode unless otherwise specified.

Items	**Contents**			
Specification	IEEE802.11b-2.4GHz			
Mode	DSSS / CCK			
Channel frequency (spacing)	2412 to 2472 MHz (5MHz)			
Data rate	1, 2, 5.5,11Mbps			
Current Consumption	**Min.**	**Typ.**	**Max.**	**Unit**
(a) Tx mode	-	370	470	mA
(b) Rx mode	-	100	150	mA
Transmitter	**Min.**	**Typ.**	**Max.**	**Unit**
Power Levels	14.5	17	19.5	dBm
Spectrum Mask				
(a) 1st side lobes	-	-	-30	dBr
(b) 2nd side lobes	-	-	-50	dBr
Power-on/off ramp	-	-	2.0	usec
RF Carrier Suppression	15	-	-	dB
Modulation Accuracy	-	-	35	%
Frequency tolerance	-20	-	20	ppm
Spurious Emissions (BW=100kHz)				
(a) 30Hz≦f<1000MHz	-	-	-36	dBm
(b) 1000MHz≦f<12750MHz	-	-	-30	dBm
(c) 1800MHz<f≦1900MHz	-	-	-47	dBm
(d) 5150MHz<f≦5300MHz	-	-	-47	dBm
Receiver	**Min.**	**Typ.**	**Max.**	**Unit**
Minimum Input Level (FER≤ 8%)	-	-	-76	dBm
Maximum Input Level (FER ≤ 8%)	-10	-	-	dBm
Adjacent Channel Rejection (FER ≤ 8%)	35	-	-	dB

14.2. DC/RF Characteristics for IEEE802.11g - 2.4G

Normal Condition : 25deg.C, VBAT =3.3V.
54Mbps mode unless otherwise specified.

Items	**Contents**			
Specification	IEEE802.11g-2.4GHz			
Mode	OFDM			
Channel frequency (spacing)	2412 to 2472 MHz (5MHz)			
Data rate	6, 9, 12, 18, 24, 36, 48, 54Mbps			
Current Consumption	**Min.**	**Typ.**	**Max.**	**unit**
(a) Tx mode	-	330	430	mA
(b) Rx mode	-	100	150	mA
Transmitter	**Min.**	**Typ.**	**Max.**	**unit**
Power Levels	12.5	15	17.5	dBm
Spectrum Mask				
(a) at fc +/- 11MHz	-	-	-20	dBr
(b) at fc +/- 20MHz	-	-	-28	dBr
(c) at fc ≥ +/-30MHz	-	-	-40	dBr
Constellation Error	-	-	-25	dB
Frequency tolerance	-20		20	ppm
Spurious Emissions (BW=100kHz)				
(a) 30Hz≦f<1000MHz	-	-	-36	dBm
(b) 1000MHz≦f<12750MHz	-	-	-30	dBm
(c) 1800MHz<f≦1900MHz	-	-	-47	dBm
(d) 5150MHz<f≦5300MHz	-	-	-47	dBm
Receiver	**Min.**	**Typ.**	**Max.**	**unit**
Minimum Input Level (PER ≤ 10%)	-	-	-65	dBm
Maximum Input Level (PER ≤ 10%)	-20	-	-	dBm
Adjacent Channel Rejection (PER ≤ 10%)	-1	-	-	dB

14.3. DC/RF Characteristics for IEEE802.11n - 2.4GHz

Normal Condition : 25deg.C, VBAT =3.3V.
65Mbps (MCS7 – HT 20MHz) mode unless otherwise specified.

Items	**Contents**			
Specification	IEEE802.11n-2.4GHz			
Mode	OFDM			
Channel frequency (spacing)	2412 to 2472 MHz (5MHz)			
Data rate	6.5, 13, 19.5, 26, 39, 52, 58.5, 65Mbps			
Current Consumption	**Min.**	**Typ.**	**Max.**	**unit**
(a) Tx mode	-	330	430	mA
(b) Rx mode	-	100	150	mA
Transmitter	**Min.**	**Typ.**	**Max.**	**unit**
Power Levels	12.5	15	17.5	dBm
Spectrum Mask				
(a) at fc +/- 11MHz	-	-	-20	dBr
(b) at fc +/- 20MHz	-	-	-28	dBr
(c) at fc ≥ +/-30MHz	-	-	-45	dBr
Constellation Error (measured at enhanced mode)	-	-	-27	dB
Frequency tolerance	-20	-	20	ppm
Spurious Emissions (BW=100kHz)				
(a) 30Hz≦f<1000MHz	-	-	-36	dBm
(b) 1000MHz≦f<12750MHz	-	-	-30	dBm
(c) 1800MHz<f≦1900MHz	-	-	-47	dBm
(d) 5150MHz<f≦5300MHz	-	-	-47	dBm
Receiver	**Min.**	**Typ.**	**Max.**	**unit**
Minimum Input Level (PER ≤ 10%)	-	-	-64	dBm
Maximum Input Level (PER ≤ 10%)	-20	-	-	dBm
Adjacent Channel Rejection (PER ≤ 10%)	-2	-	-	dB

14.4. DC/RF Characteristics for IEEE802.11a - 5GHz

Normal Condition : 25deg.C, VBAT =3.3V.
54Mbps mode unless otherwise specified.

Items	**Contents**			
Specification	IEEE802.11a-5GHz			
Mode	OFDM			
Channel frequency (spacing)	5180 - 5825MHz			
Data rate	6, 9, 12, 18, 24, 36, 48, 54Mbps			
Current Consumption	**Min.**	**Typ.**	**Max.**	**Unit**
(a) Tx mode	-	400	500	mA
(b) Rx mode	-	120	170	mA
Transmitter	**Min.**	**Typ.**	**Max.**	**Unit**
Power Levels	11.5	14	16.5	dBm
Spectrum Mask				
(a) at fc +/- 11MHz	-	-	-20	dBr
(b) at fc +/- 20MHz	-	-	-28	dBr
(c) at fc ≥ +/-30MHz	-	-	-40	dBr
Constellation Error	-	-	-25	dB
Frequency tolerance	-20		20	ppm
Spurious Emissions (BW=100kHz)				
(a) 30Hz≦f<1000MHz	-	-	-36	dBm
(b) 1000MHz≦f<26000MHz	-	-	-30	dBm
Receiver	**Min.**	**Typ.**	**Max.**	**Unit**
Minimum Input Level (PER ≤ 10%)	-	-	-65	dBm
Maximum Input Level (PER ≤ 10%)	-30	-	-	dBm
Adjacent Channel Rejection (PER < 10%)	-1			dB

14.5. DC/RF Characteristics for IEEE802.11n(HT 20MHz) - 5GHz

Normal Condition : 25deg.C, VBAT =3.3V.
65Mbps (MCS7 – HT 20MHz) mode unless otherwise specified.

Items	**Contents**			
Specification	IEEE802.11n-5GHz			
Mode	OFDM			
Channel frequency (spacing)	5180 - 5825MHz			
Data rate	6.5, 13, 19.5, 26, 39, 52, 58.5, 65Mbps			
Current Consumption	**Min.**	**Typ.**	**Max.**	**Unit**
(a) Tx mode	-	380	480	mA
(b) Rx mode	-	120	170	mA
Transmitter	**Min.**	**Typ.**	**Max.**	**Unit**
Power Levels	10.5	13	15.5	dBm
Spectrum Mask				
(a) at fc +/- 11MHz	-	-	-20	dBr
(b) at fc +/- 20MHz	-	-	-28	dBr
(c) at fc ≥ +/-30MHz	-	-	-40	dBr
Constellation Error (measured at enhanced mode)	-	-	-27	dB
Frequency tolerance	-20		20	ppm
Spurious Emissions (BW=100kHz)				
(a) 30Hz≦f<1000MHz	-	-	-36	dBm
(b) 1000MHz≦f<26000MHz	-	-	-30	dBm
Receiver	**Min.**	**Typ.**	**Max.**	**Unit**
Minimum Input Level (PER ≤ 10%)	-	-	-64	dBm
Maximum Input Level (PER ≤ 10%)	-30	-	-	dBm
Adjacent Channel Rejection (PER < 10%)	16	-	-	dB

14.6. DC/RF Characteristics for IEEE802.11n(HT 40MHz) - 5GHz

Normal Condition : 25deg.C, VBAT =3.3V.
135Mbps (MCS7 – HT 40MHz) mode unless otherwise specified.

Items	**Contents**			
Specification	IEEE802.11n-5GHz			
Mode	OFDM			
Channel frequency (spacing)	5180 - 5825MHz			
Data rate	13.5,27,40.5,54,81,108,121.5,135Mbps			
Current Consumption	**Min.**	**Typ.**	**Max.**	**Unit**
(a) Tx mode	-	410	510	mA
(b) Rx mode	-	140	190	mA
Transmitter	**Min.**	**Typ.**	**Max.**	**Unit**
Power Levels	9.5	12	14.5	dBm
Spectrum Mask				
(a) at fc +/- 21MHz	-	-	-20	dBr
(b) at fc +/- 40MHz	-	-	-28	dBr
(c) at fc ≥ +/-60MHz	-	-	-40	dBr
Constellation Error (measured at enhanced mode)	-	-	-27	dB
Frequency tolerance	-20		20	ppm
Spurious Emissions (BW=100kHz)				
(a) 30Hz≦f<1000MHz	-	-	-36	dBm
(b)1000MHz≦f<26000MHz	-	-	-30	dBm
Receiver	**Min.**	**Typ.**	**Max.**	**Unit**
Minimum Input Level (PER ≤ 10%)	-	-	-61	dBm
Maximum Input Level (PER ≤ 10%)	-30	-	-	dBm
Adjacent Channel Rejection (PER < 10%)	-2			dB

14.7. DC/RF Characteristics for IEEE802.11ac(HT 40MHz) - 5GHz

Normal Condition : 25deg.C, VBAT =3.3V.
180Mbps (MCS9 – HT 40MHz) mode unless otherwise specified.

Items	**Contents**			
Specification	IEEE802.11ac-5GHz			
Mode	OFDM			
Channel frequency (spacing)	5190 - 5795MHz			
Data rate	13.5,27,40.5,54,81,108,121.5,135,162,180Mbps			
Current Consumption	**Min.**	**Typ.**	**Max.**	**Unit**
(a) Tx mode	-	420	520	mA
(b) Rx mode	-	140	200	mA
Transmitter	**Min.**	**Typ.**	**Max.**	**Unit**
Power Levels	7.5	10	12.5	dBm
Spectrum Mask				
(a) at fc +/- 21MHz	-	-	-20	dBr
(b) at fc +/- 40MHz	-	-	-28	dBr
(c) at fc ≥ +/-60MHz	-	-	-40	dBr
Constellation Error (measured at enhanced mode)	-	-	-32	dB
Frequency tolerance	-20		20	ppm
Spurious Emissions (BW=100kHz)				
(a) 30Hz≦f<1000MHz	-	-	-36	dBm
(b) 1000MHz≦f<26000MHz	-	-	-30	dBm
Receiver	**Min.**	**Typ.**	**Max.**	**Unit**
Minimum Input Level (PER ≤ 10%)	-	-	-54	dBm
Maximum Input Level (PER ≤ 10%)	-30	-	-	dBm

14.8. DC/RF Characteristics for IEEE802.11ac(HT 80MHz) - 5GHz

Normal Condition : 25deg.C, VBAT =3.3V.
390Mbps (MCS9 – HT 80MHz) mode unless otherwise specified.

Items	**Contents**			
Specification	IEEE802.11ac-5GHz			
Mode	OFDM			
Channel frequency (spacing)	5210 - 5775MHz			
Data rate	29.3,58.5,87.8,117,175.5,234,263.3,292.5,351,390 Mbps			
Current Consumption	**Min.**	**Typ.**	**Max.**	**Unit**
(a) Tx mode	-	440	540	mA
(b) Rx mode	-	180	250	mA
Transmitter	**Min.**	**Typ.**	**Max.**	**Unit**
Power Levels	7.5	10	12.5	dBm
Spectrum Mask				
(a) at fc +/- 41MHz	-	-	-20	dBr
(b) at fc +/- 80MHz	-	-	-28	dBr
(c) at fc ≥ +/-120MHz	-	-	-40	dBr
Constellation Error (measured at enhanced mode)	-	-	-32	dB
Spurious Emissions (BW=100kHz)				
(a) 30Hz≦f<1000MHz	-	-	-36	dBm
(b)1000MHz≦f<26000MHz	-	-	-30	dBm
Receiver	**Min.**	**Typ.**	**Max.**	**Unit**
Minimum Input Level (PER ≤ 10%)	-	-	-51	dBm
Maximum Input Level (PER ≤ 10%)	-30	-	-	dBm
Adjacent Channel Rejection (PER < 10%)	-9			dB

14.9. DC/RF Characteristics for Bluetooth

Normal conditions : 25 deg.C, VBAT = 3.3V

Items	Contents			
Bluetooth specification (power class)	Version 5.2 (Class2)			
Channel frequency (spacing)	2402 to 2480 MHz (1MHz)			
Current Consumption	**Min.**	**Typ.**	**Max.**	**unit**
(a) DH5 Packet 50% Rx/Tx slot duty cycle	-	50	65	mA
(b) 2DH5 Packet 50% Rx/Tx slot duty cycle	-	40	55	mA
(c) 3DH5 Packet 50% Rx/Tx slot duty cycle	-	40	45	mA
Transmitter	**Min.**	**Typ.**	**Max.**	**Unit**
Output Power (at 1DH5)	7.5	11	14.5	dBm
Frequency range	2400	-	2483.5	MHz
20dB bandwidth	-		1	MHz
Adjacent Channel Power *1				
(a) [M-N] =2	-	-	-20	dBm
(b) [M-N] ≥3	-	-	-40	dBm
Modulation characteristics				
(a) Modulation Δf1avg	140	-	175	kHz
(b) Modulation Δf2max	115		-	kHz
(c) Modulation Δf2avg / Δf1avg	0.8	-	-	
Carrier Frequency Drift				
(a) 1slot	-25	-	+25	kHz
(b) 3slot / 5slot	-40	-	+40	kHz
(c) Maximum drift rate	-20	-	+20	kHz/50us
EDR Relative Power	-4	-	+1	dB
EDR Carrier Frequency Stability and Modulation Accuracy				
(a) ωi	-75	-	+75	kHz
(b) ωi+ωo	-75	-	+75	kHz
(c) ωo	-10	-	+10	kHz
(d) RMS DEVM (DQPSK)	-	-	20	%
(e) Peak DEVM (DQPSK)	-	-	35	%
(f) 99% DEVM (DQPSK)	-	-	30	%
(g) RMS DEVM (8DPSK)	-	-	13	%
(h) Peak DEVM (8DPSK)	-	-	25	%
(i) 99% DEVM (8DPSK)	-	-	20	%
Spurious Emissions (BW=100kHz)				
(a) 30Hz≦f<1000MHz	-	-	-36	dBm
(b)1000MHz≦f<12750MHz	-	-	-30	dBm
(c) 1800MHz<f≦1900MHz	-	-	-47	dBm
(d) 5150MHz<f≦5300MHz	-	-	-47	dBm
Receiver	**Min.**	**Typ.**	**Max.**	**unit**
Sensitivity (BER≤0.1%)	-	-	-80	dBm
Maximum Input Level (BER≤0.1%)	-20	-	-	dBm
EDR Sensitivity (BER≤0.007%)				
(a) 8DPSK	-	-	-70	dBm

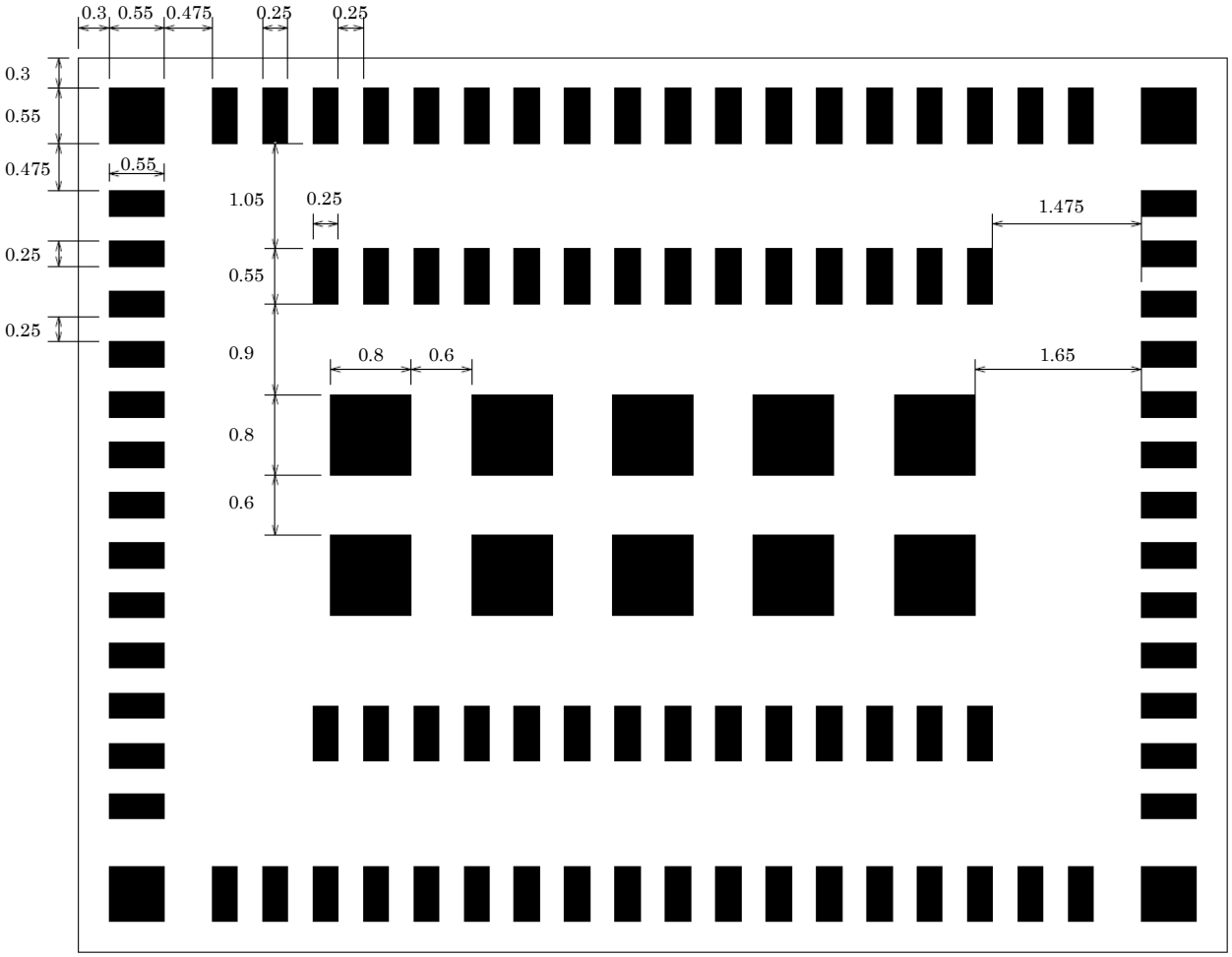
*1: Up to three spurious responses within Bluetooth limits are allowed.

14.10. DC/RF Characteristics for Bluetooth (LE)

Conditions : 25deg.C, VBAT=3.3V

Items	**Contents**			
Bluetooth specification (power class)	Version 5.2(LE)			
Channel frequency (spacing)	2402 to 2480 MHz (2MHz)			
Number of RF Channel	40			
Current Consumption	**Min.**	**Typ.**	**Max.**	**Unit**
(a) Tx mode	-	30	45	mA
(b) Rx mode	-	15	25	mA
Item / Condition	**Min.**	**Typ.**	**Max.**	**Unit**
Center Frequency	2402	-	2480	MHz
Channel Spacing	-	2	-	MHz
Number of RF channel	-	40	-	-
Output power	0	3	7.5	dBm
Modulation Characteristics				
1) $\Delta f1_{avg}$	225	-	275	kHz
2) $\Delta f2_{max}$ (at 99.9%)	185	-	-	kHz
3) $\Delta f2_{avg}$ / $\Delta f1_{avg}$	0.8	-	-	-
Carrier frequency offset and drift				
1) Frequency offset	-	-	150	kHz
2) Frequency drift	-	-	50	kHz
3) Drift rate	-	-	20	kHz
Receiver sensitivity (PER < 30.8%)	-	-	-70	dBm
Maximum input signal level (PER < 30.8%)	-10	-	-	dBm
PER Report Integrity (-30dBm input)	50	-	65.4	%

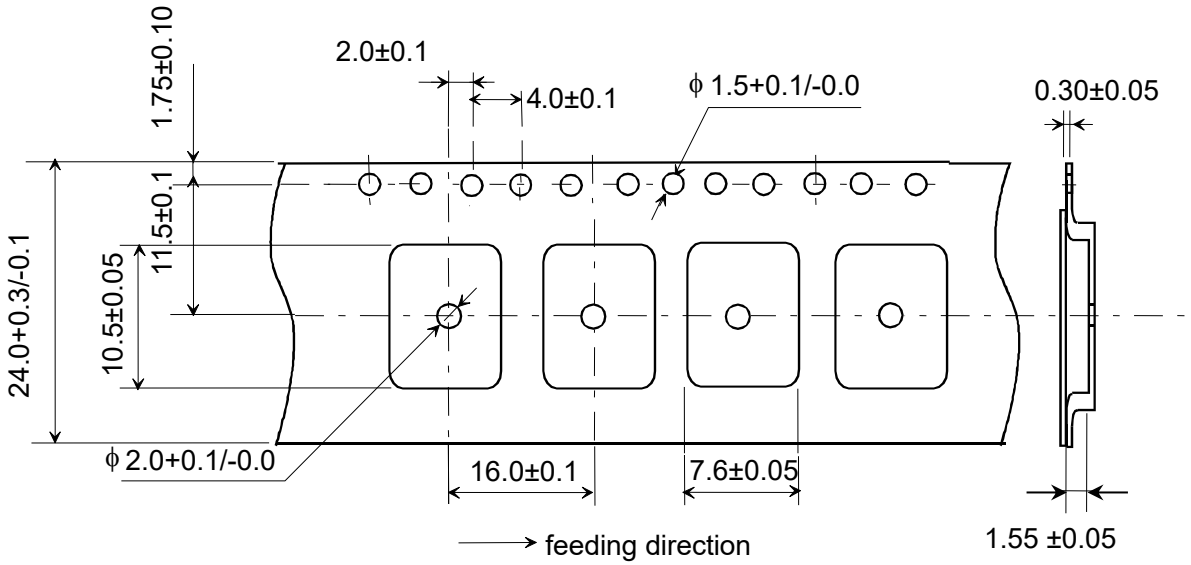
15. Land Pattern



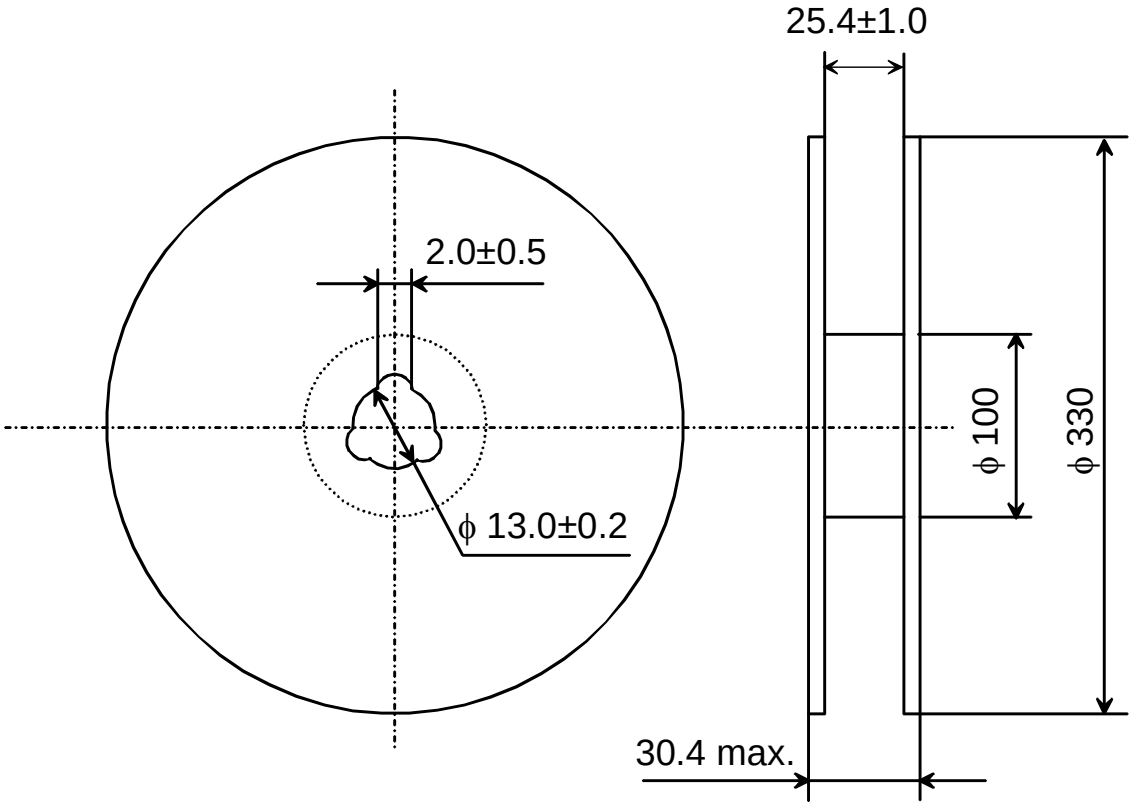
Top View. Unit : mm

16. TAPE AND REEL PACKING

(1) Dimensions of Tape (Plastic tape)

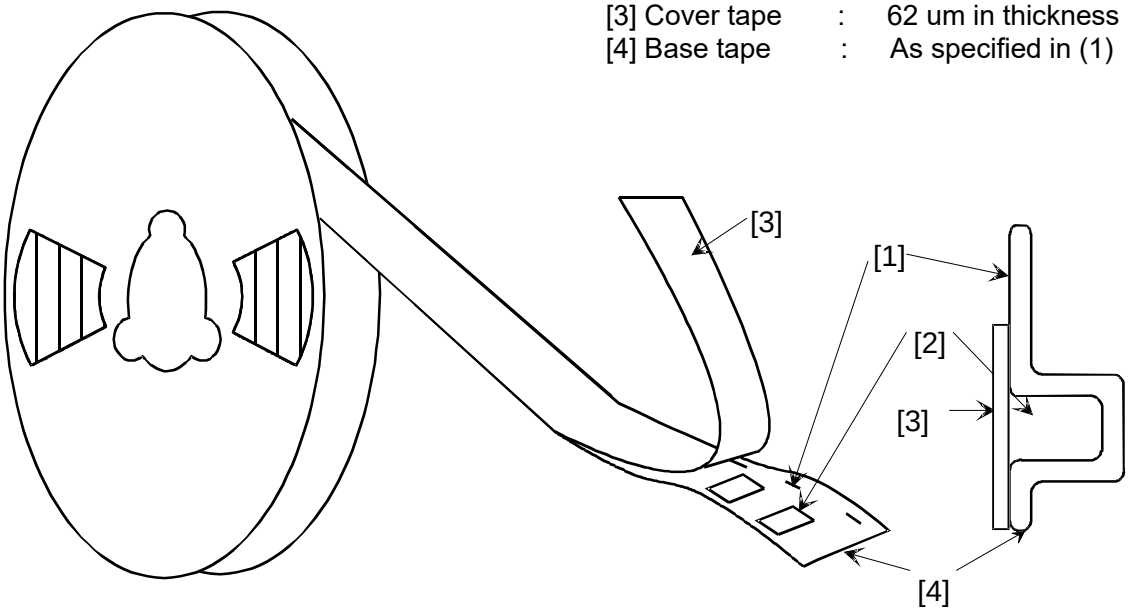


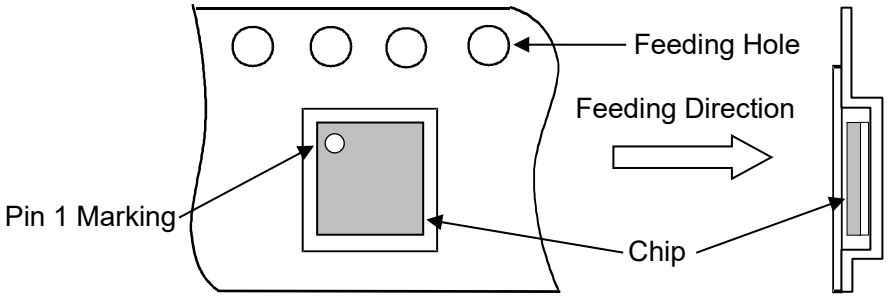
(2) Dimensions of Reel



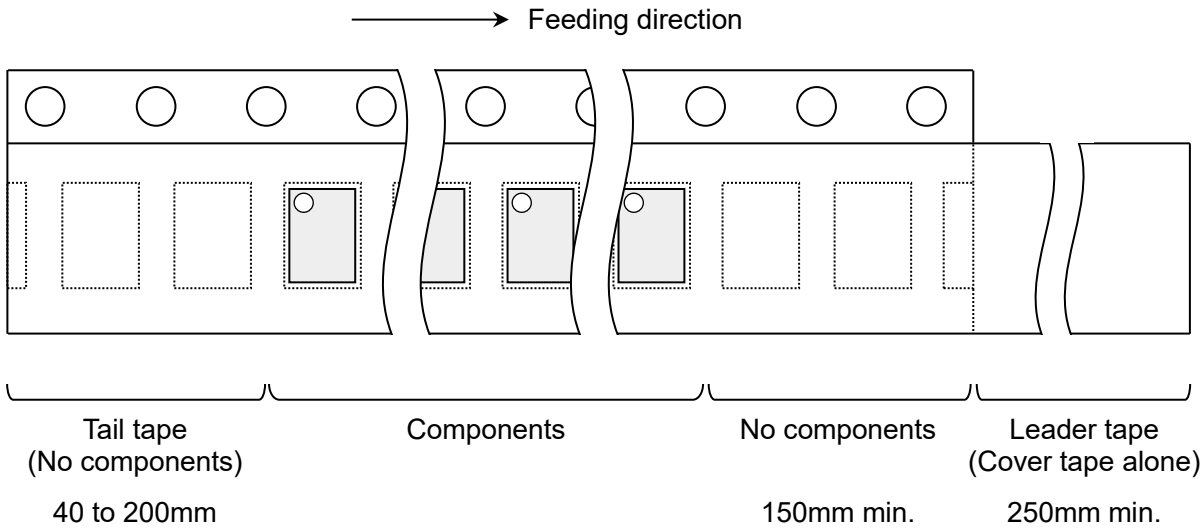
(3) Taping Diagrams

[1] Feeding Hole : As specified in (1)
[2] Hole for chip : As specified in (1)
[3] Cover tape : 62 um in thickness
[4] Base tape : As specified in (1)





(4) Leader and Tail tape



(5) The tape for chips are wound clockwise, the feeding holes to the right side as the tape is pulled toward the user.

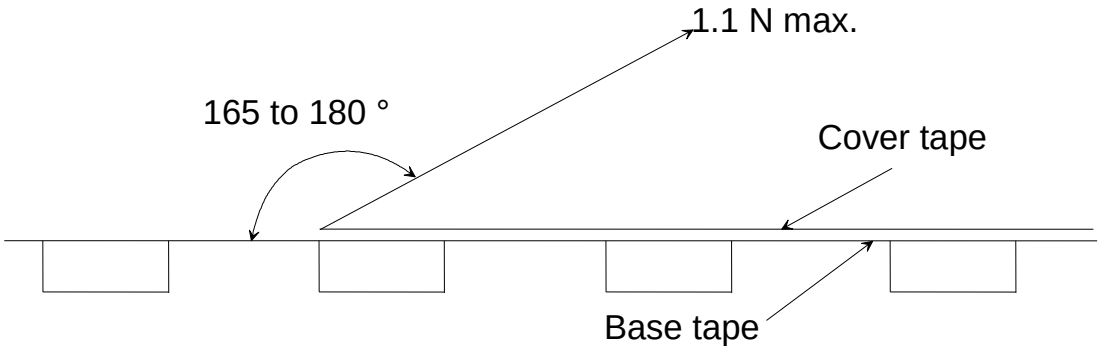
(6) The cover tape and base tape are not adhered at no components area for 250mm min.

(7) Tear off strength against pulling of cover tape: 5N min.

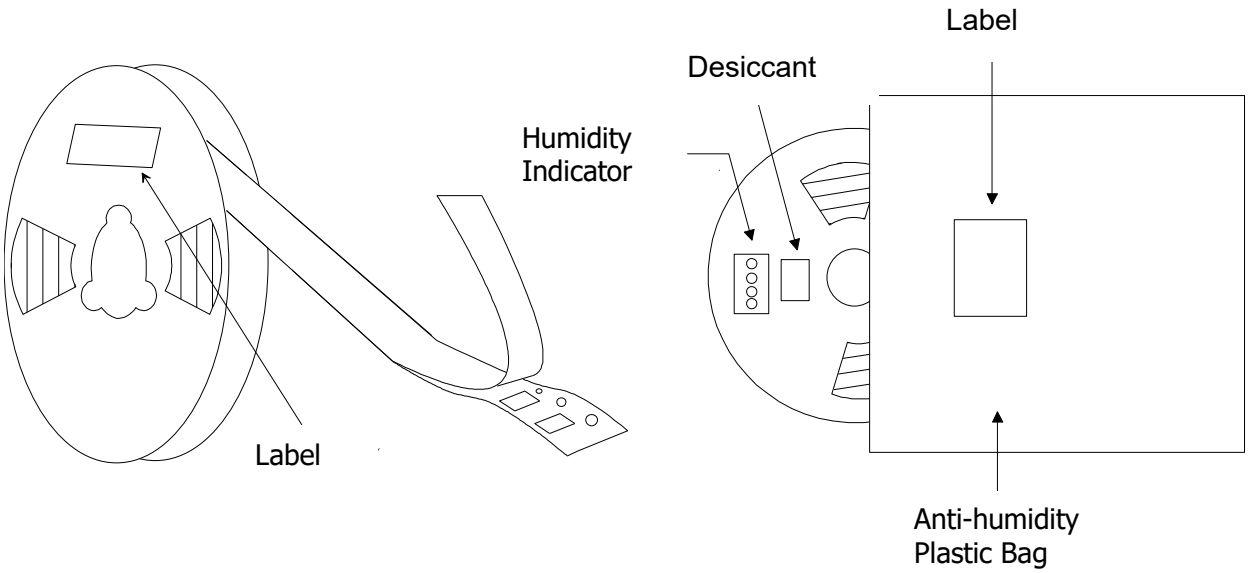
(8) Packaging unit : 1000pcs./ reel

(9) material - Base tape : Plastic
Reel : Plastic
Cover tape, cavity tape and reel are made the anti-static processing.

(10) Peeling of force: 1.1N max. in the direction of peeling as shown below.



(11) PACKAGE (Humidity proof packing)



Tape and reel must be sealed with the anti-humidity plastic bag. The bag contains the desiccant and the humidity indicator.

17. NOTICE

17.1. Storage Conditions:

Please use this product within 6month after receipt.
- The product shall be stored without opening the packing under the ambient temperature from 5 to 35deg.C and humidity from 20 to 70%RH.
(Packing materials, in particular, may be deformed at the temperature over 40deg.C.)
- The product left more than 6months after reception, it needs to be confirmed the solderbility before used.
- The product shall be stored in non corrosive gas (Cl_2, NH_3, SO_2, No_x, etc.).
- Any excess mechanical shock including, but not limited to, sticking the packing materials by sharp object and dropping the product, shall not be applied in order not to damage the packing materials.

This product is applicable to MSL3 (Based on JEDEC Standard J-STD-020)
- After the packing opened, the product shall be stored at ≦30deg.C / ≦60%RH and the product shall be used within 168hours.
- When the color of the indicator in the packing changed, the product shall be baked before soldering.

Baking condition: 125+5/-0deg.C, 24hours, 1time
The products shall be baked on the heat-resistant tray because the material (Base Tape, Reel Tape and Cover Tape) are not heat-resistant.

17.2. Handling Conditions:

Be careful in handling or transporting products because excessive stress or mechanical shock may break products.

Handle with care if products may have cracks or damages on their terminals, the characteristics of products may change. Do not touch products with bear hands that may result in poor solder ability and destroy by static electrical charge.

17.3. Standard PCB Design (Land Pattern and Dimensions):

All the ground terminals should be connected to the ground patterns. Furthermore, the ground pattern should be provided between IN and OUT terminals. Please refer to the specifications for the standard land dimensions.

The recommended land pattern and dimensions is as Murata's standard. The characteristics of products may vary depending on the pattern drawing method, grounding method, land dimensions, land forming method of the NC terminals and the PCB material and thickness. Therefore, be sure to verify the characteristics in the actual set. When using non-standard lands, contact Murata beforehand.

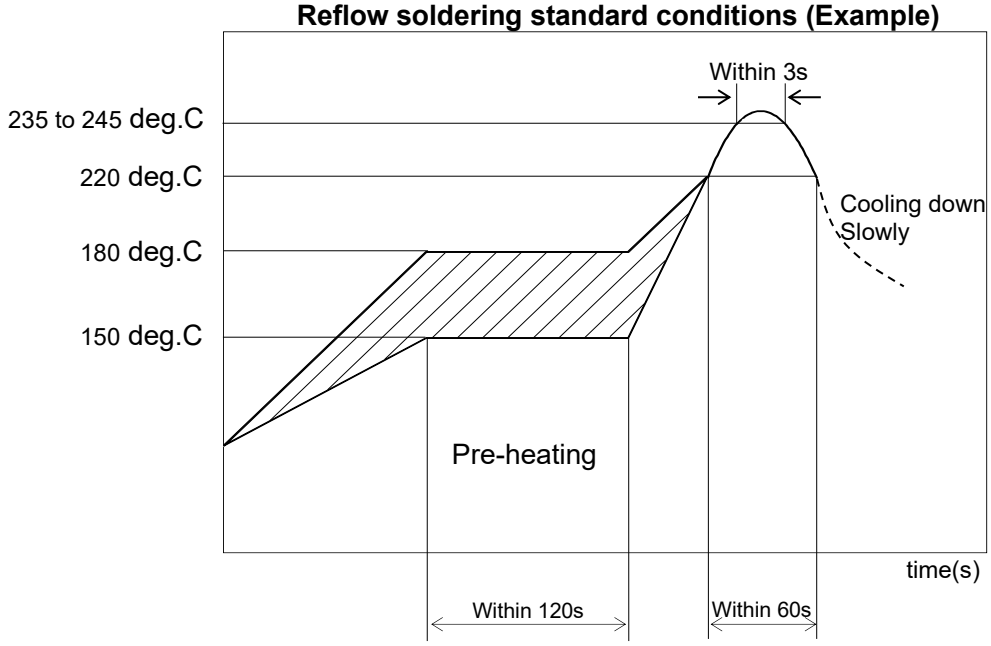
17.4. Notice for Chip Placer:

When placing products on the PCB, products may be stressed and broken by uneven forces from a worn-out chucking locating claw or a suction nozzle. To prevent products from damages, be sure to follow the specifications for the maintenance of the chip placer being used. For the positioning of products on the PCB, be aware that mechanical chucking may damage products.

17.5. Soldering Conditions:

The recommendation conditions of soldering are as in the following figure.
Soldering must be carried out by the above mentioned conditions to prevent products from damage.
Set up the highest temperature of reflow within 260 °C. Contact Murata before use if concerning other soldering conditions.

Reflow soldering standard conditions (Example)



Please use the reflow within 2 times.
Use rosin type flux or weakly active flux with a chlorine content of 0.2 wt % or less.

17.6. Cleaning:

Since this Product is Moisture Sensitive, any cleaning is not recommended. If any cleaning process is done the customer is responsible for any issues or failures caused by the cleaning process.

17.7. Operational Environment Conditions:

Products are designed to work for electronic products under normal environmental conditions (ambient temperature, humidity and pressure). Therefore, products have no problems to be used under the similar conditions to the above-mentioned. However, if products are used under the following circumstances, it may damage products and leakage of electricity and abnormal temperature may occur.

- In an atmosphere containing corrosive gas (Cl_2, NH_3, SO_x, NO_x etc.).
- In an atmosphere containing combustible and volatile gases.
- Dusty place.
- Direct sunlight place.
- Water splashing place.
- Humid place where water condenses.
- Freezing place.

If there are possibilities for products to be used under the preceding clause, consult with Murata before actual use.

As it might be a cause of degradation or destruction to apply static electricity to products, do not apply static electricity or excessive voltage while assembling and measuring.

17.8. Input Power Capacity:

Products shall be used in the input power capacity as specified in this specifications.
Inform Murata beforehand, in case that the components are used beyond such input power capacity range.

18. PRECONDITION TO USE OUR PRODUCTS

PLEASE READ THIS NOTICE BEFORE USING OUR PRODUCTS.

Please make sure that your product has been evaluated and confirmed from the aspect of the fitness for the specifications of our product when our product is mounted to your product.
All the items and parameters in this product specification/datasheet/catalog have been prescribed on the premise that our product is used for the purpose, under the condition and in the environment specified in this specification. You are requested not to use our product deviating from the condition and the environment specified in this specification.
Please note that the only warranty that we provide regarding the products is its conformance to the specifications provided herein. Accordingly, we shall not be responsible for any defects in products or equipment incorporating such products, which are caused under the conditions other than those specified in this specification.
WE HEREBY DISCLAIMS ALL OTHER WARRANTIES REGARDING THE PRODUCTS, EXPRESS OR IMPLIED, INCLUDING WITHOUT LIMITATION ANY WARRANTY OF FITNESS FOR A PARTICULAR PURPOSE, THAT THEY ARE DEFECT-FREE, OR AGAINST INFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS.
The product shall not be used in any application listed below which requires especially high reliability for the prevention of such defect as may directly cause damage to the third party's life, body or property. You acknowledge and agree that, if you use our products in such applications, we will not be responsible for any failure to meet such requirements. Furthermore, YOU AGREE TO INDEMNIFY AND DEFEND US AND OUR AFFILIATES AGAINST ALL CLAIMS, DAMAGES, COSTS, AND EXPENSES THAT MAY BE INCURRED, INCLUDING WITHOUT LIMITATION, ATTORNEY FEES AND COSTS, DUE TO THE USE OF OUR PRODUCTS IN SUCH APPLICATIONS.

- Aircraft equipment.
- Aerospace equipment
- Undersea equipment.
- Power plant control equipment
- Medical equipment.
- Traffic signal equipment.
- Burning / explosion control equipment
- Disaster prevention / crime prevention equipment.
- Transportation equipment (vehicles, trains, ships, elevator, etc.).
- Application of similar complexity and/ or reliability requirements to the applications listed in the above.

We expressly prohibit you from analyzing, breaking, reverse-engineering, remodeling altering, and reproducing our product.
Our product cannot be used for the product which is prohibited from being manufactured, used, and sold by the regulations and laws in the world.
We do not warrant or represent that any license, either express or implied, is granted under any our patent right, copyright, mask work right, or our other intellectual property right relating to any combination, machine, or process in which our products or services are used. Information provided by us regarding third-party products or services does not constitute a license from us to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from us under our patents or other intellectual property.
Please do not use our products, our technical information and other data provided by us for the purpose of developing of mass-destruction weapons and the purpose of military use.
Moreover, you must comply with "foreign exchange and foreign trade law", the "U.S. export administration regulations", etc.
Please note that we may discontinue the manufacture of our products, due to reasons such as end of supply of materials and/or components from our suppliers.
By signing on specification sheet or approval sheet, you acknowledge that you are the legal representative for your company and that you understand and accept the validity of the contents herein. When you are not able to return the signed version of specification sheet or approval sheet within 30 days from receiving date of specification sheet or approval sheet, it shall be deemed to be your consent on the content of specification sheet or approval sheet. Customer acknowledges that engineering samples may deviate from specifications and may contain defects due to their development status. We reject any liability or product warranty for engineering samples. In particular we disclaim liability for damages caused by
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-deviation or lapse in function of engineering sample,
-improper use of engineering samples.
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