N-Channel Power MOSFET 600 V, 745 m Ω

Features

- 100% Avalanche Tested
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS

ABSOLUTE MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	600	V
Gate-to-Source Vo	ltage		V_{GS}	±25	V
Continuous Drain	Steady	T _C = 25°C	I _D	6.6	Α
Current R _{θJC}	State	T _C = 100°C		4.2	
Power Dissipation - R ₀ JC	Steady State	T _C = 25°C	P _D	84	W
Pulsed Drain Current	t _p = 10 μs		I _{DM}	27	Α
Operating Junction and Storage Temperature			T _J , T _{STG}	-55 to +150	°C
Source Current (Body Diode)			IS	6.6	Α
Single Pulse Drain-to-Source Avalanche Energy (I _D = 2.5 A)			EAS	38	mJ
Peak Diode Recovery (Note 1)			dv/dt	15	V/ns
Lead Temperature for	or Solderin	g Leads	T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected. 1. $I_{SD} < 6.6$ A, di/dt \leq 400 A/ μ s, V_{DS} peak \leq $V_{(BR)DSS}$, $V_{DD} = 80\%$ $V_{(BR)DSS}$

THERMAL RESISTANCE

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain) NDD60N745U1	$R_{ heta JC}$	1.5	°C/W
Junction-to-Ambient Steady State (Note 3) NDD60N745U1 (Note 2) NDD60N745U1-1 (Note 2) NDD60N745U1-35	$R_{ hetaJA}$	47 98 95	°C/W

- 2. Insertion mounted
- 3. Surface mounted on FR4 board using 1" sq. pad size (Cu area = 1.127 in sq [2 oz] including traces)

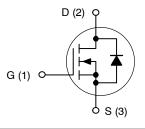


ON Semiconductor®

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V _{(BR)DSS}	R _{DS(ON)} MAX
600 V	745 mΩ @ 10 V

N-Channel MOSFET





STYLE 2



DPAK CASE 369C STYLE 2



CASE 369AD STYLE 2

ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Test Conditions	s	Min	Тур	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 1 r	mA	600			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J				540		mV/°C
Drain-to-Source Leakage Current	I _{DSS}	V _{DS} = 600 V, V _{GS} = 0 V	T _J = 25°C			1	μΑ
			T _J = 125°C			100	1
Gate-to-Source Leakage Current	I _{GSS}	V _{GS} = ±20 V				±100	nA
ON CHARACTERISTICS (Note 4)			-				
Gate Threshold Voltage	V _{GS(TH)}	$V_{DS} = V_{GS}, I_{D} = 250$	0 μΑ	2	3.2	4	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J	Reference to 25°C, I _D =	= 250 μA		7.6		mV/°C
Static Drain-to-Source On Resistance	R _{DS(on)}	$V_{GS} = 10 \text{ V}, I_D = 3.2$	25 A		610	745	mΩ
Forward Transconductance	9FS	$V_{DS} = 15 \text{ V}, I_D = 3.2$	25 A		5.6		S
DYNAMIC CHARACTERISTICS			-				
Input Capacitance	C _{iss}				440		pF
Output Capacitance	C _{oss}	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}, f$	= 1 MHz		27		1
Reverse Transfer Capacitance	C _{rss}				1.5		1
Effective output capacitance, energy related (Note 6)	C _{o(er)}	V _{GS} = 0 V, V _{DS} = 0 to 480 V			21]
Effective output capacitance, time related (Note 7)	C _{o(tr)}	I_D = constant, V_{GS} = 0 V, V_{DS} = 0 to 480 V			71]
Total Gate Charge	Q_g				15		nC
Gate-to-Source Charge	Q_{gs}		, ,,,,,		2.9		1
Gate-to-Drain Charge	Q _{gd}	$V_{DS} = 300 \text{ V}, I_D = 6.8 \text{ A}, V_{DS} = 6.8 \text{ A}$	/ _{GS} = 10 V		7.3		1
Plateau Voltage	V_{GP}		•		5.3		V
Gate Resistance	R_g				4.4		Ω
RESISTIVE SWITCHING CHARACTER)				•	
Turn-on Delay Time	t _{d(on)}				8		ns
Rise Time	t _r	V _{DD} = 300 V, I _D = 6.	.8 A.		10		1
Turn-off Delay Time	t _{d(off)}	$V_{GS} = 10 \text{ V}, R_G = 0$	0 Ω		19		1
Fall Time	t _f	1			7		1
SOURCE-DRAIN DIODE CHARACTER					-	-	
Diode Forward Voltage	V_{SD}	$I_S = 6.6 \text{ A}, V_{GS} = 0 \text{ V}$ $T_J = 25^{\circ}\text{C}$ $T_J = 100^{\circ}\text{C}$			0.90	1.6	V
					0.82		1
Reverse Recovery Time	t _{rr}				260		ns
Charge Time	ta	$V_{GS} = 0 \text{ V}, V_{DD} = 30 \text{ V}$ $I_{S} = 6.8 \text{ A}, d_i/d_t = 100 \text{ A}/\mu\text{s}$			130		1
Discharge Time	t _b				130		1
Reverse Recovery Charge	Q _{rr}				2.1	<u> </u>	μС

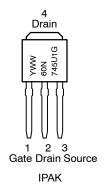
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

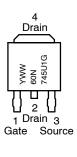
4. Pulse Width $\leq 300~\mu$ s, Duty Cycle $\leq 2\%$.

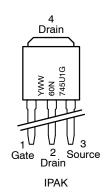
5. Switching characteristics are independent of operating junction temperatures.

6. $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$ 7. $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

MARKING DIAGRAMS







Y = Year WW = Work Week G = Pb-Free Package

DPAK

ORDERING INFORMATION

Device	Package	Shipping [†]
NDD60N745U1-1G	IPAK (Pb-Free, Halogen-Free)	75 Units / Rail
NDD60N745U1-35G	IPAK (Pb-Free, Halogen-Free)	75 Units / Rali
NDD60N745U1T4G	DPAK (Pb-Free, Halogen-Free)	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

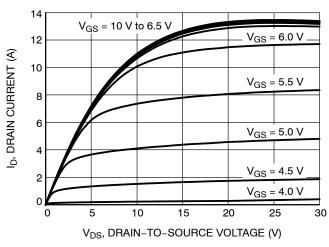


Figure 1. On-Region Characteristics

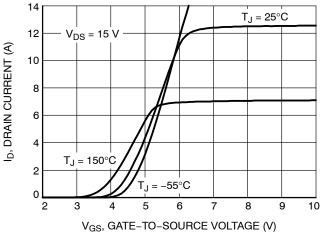


Figure 2. Transfer Characteristics

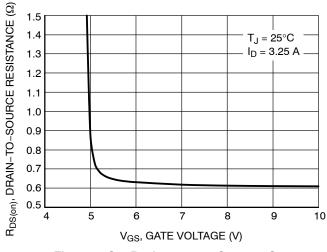


Figure 3. On-Resistance vs. Gate-to-Source Voltage

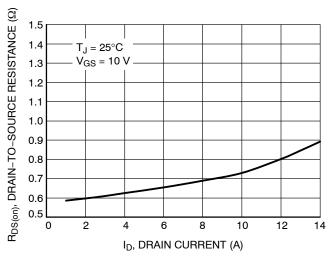


Figure 4. On–Resistance vs. Drain Current and

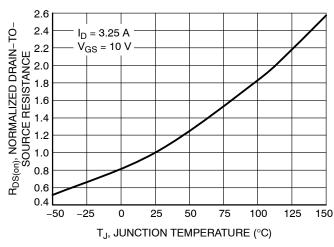


Figure 5. On–Resistance Variation with Temperature

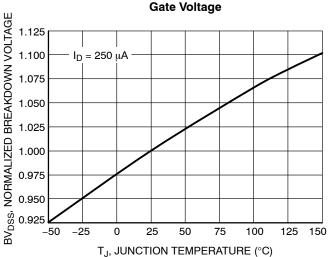


Figure 6. Breakdown Voltage Variation with Temperature

TYPICAL CHARACTERISTICS

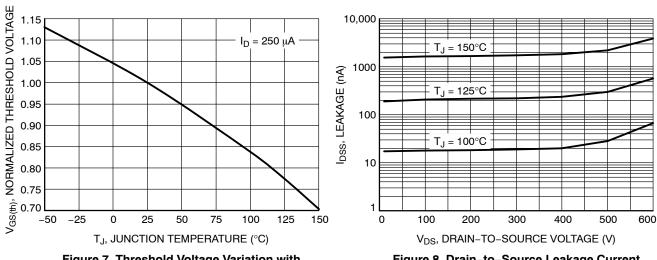


Figure 7. Threshold Voltage Variation with Temperature

Figure 8. Drain-to-Source Leakage Current vs. Voltage

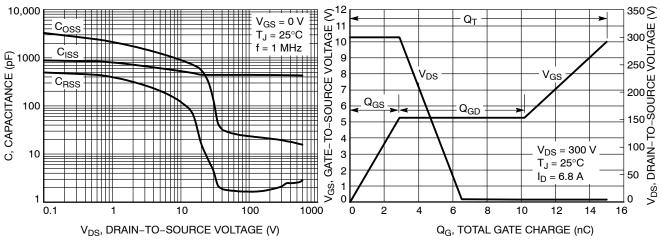


Figure 9. Capacitance Variation

Figure 10. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

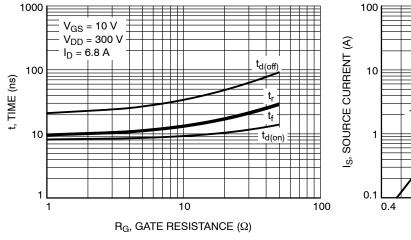


Figure 11. Resistive Switching Time Variation vs. Gate Resistance

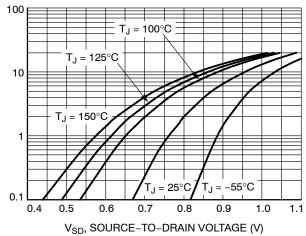


Figure 12. Diode Forward Voltage vs. Current

TYPICAL CHARACTERISTICS

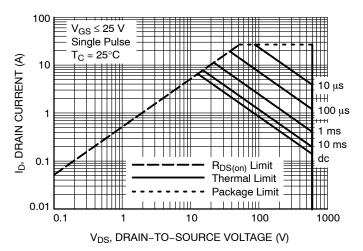


Figure 13. Maximum Rated Forward Biased Safe Operating Area

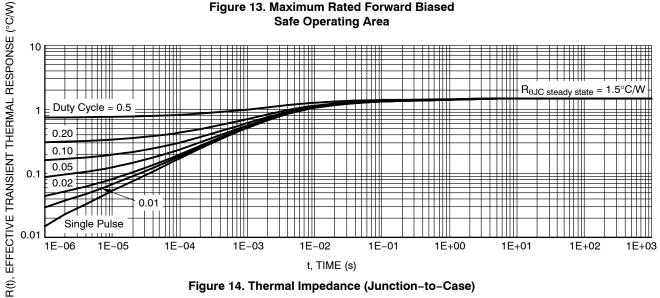


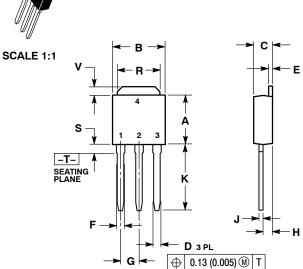
Figure 14. Thermal Impedance (Junction-to-Case)

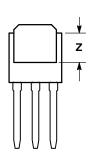
MECHANICAL CASE OUTLINE





DATE 15 DEC 2010





NOTES:

- DIMENSIONING AND TOLERANCING PER
- ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.235	0.245	5.97	6.35
В	0.250	0.265	6.35	6.73
С	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29	BSC
Н	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
٧	0.035	0.050	0.89	1.27
Z	0.155		3.93	

MARKING DIAGRAMS

STYLE 1: PIN 1. BASE 2. COLLECTOR **EMITTER** 3 COLLECTOR STYLE 6: PIN 1. MT1 2. MT2 3. GATE STYLE 5: PIN 1. GATE

2. ANODE 3. CATHODE

ANODE

STYLE 2: PIN 1. GATE 2. DRAIN SOURCE 3 4. DRAIN

MT2

4. CATHODE STYLE 7: PIN 1. GATE 2. COLLECTOR

STYLE 3: PIN 1. ANODE

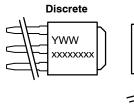
3. EMITTER COLLECTOR

2. CATHODE

3 ANODE

STYLE 4: PIN 1. CATHODE

 ANODE
 GATE 4. ANODE





xxxxxxxxx = Device Code Α = Assembly Location IL = Wafer Lot Υ = Year WW = Work Week

DOCUMENT NUMBER:	98AON10528D	Electronic versions are uncontrolled except when accessed directly from the Document Reposito Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	IPAK (DPAK INSERTION MOUNT)		PAGE 1 OF 1

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MECHANICAL CASE OUTLINE

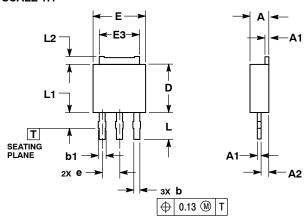


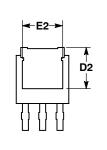
3.5 MM IPAK, STRAIGHT LEAD

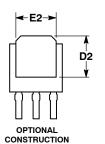
CASE 369AD **ISSUE B**

DATE 18 APR 2013









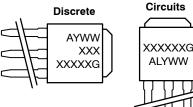
- NOTES:
 1.. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994. 2.. CONTROLLING DIMENSION: MILLIMETERS.
- DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD GATE OR MOLD FLASH.

	MILLIMETERS			
DIM	MIN MAX			
Α	2.19	2.38		
A1	0.46	0.60		
A2	0.87	1.10		
b	0.69	0.89		
b1	0.77	1.10		
D	5.97	6.22		
D2	4.80			
E	6.35	6.73		
E2	4.57	5.45		
E3	4.45	5.46		
е	2.28 BSC			
L	3.40	3.60		
L1		2.10		
L2	0.89	1.27		

GENERIC MARKING DIAGRAMS*

Integrated

Discrete





STYLE 5:

PIN 1. GATE

2. COLLECTOR 3. EMITTER

ANODE
 CATHODE

ANODE

COLLECTOR

STYLE 6:

PIN 1. MT1

MT2
 GATE

MT2

STYLE 2: PIN 1. GATE 2. DRAIN 3. SOURCE DRAIN

STYLE 3: PIN 1. ANODE 2. CATHODE 3. ANODE

CATHODE

STYLE 7: PIN 1. GATE

2. COLLECTOR 3. EMITTER COLLECTOR

STYLE 4: PIN 1. CATHODE 2. ANODE

3. GATE ANODE

> XXXXXX = Device Code

Α = Assembly Location

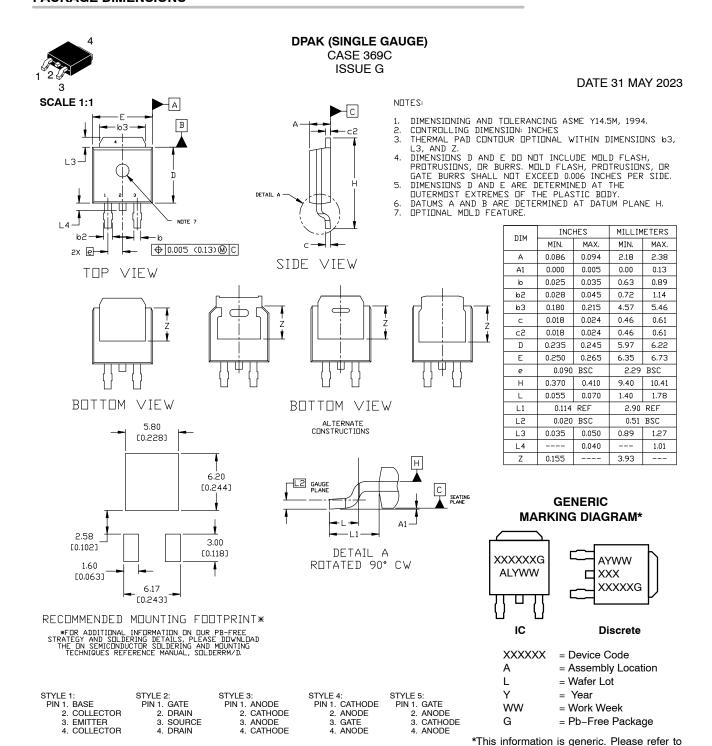
L = Wafer Lot Υ = Year WW = Work Week G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " ■", may or may not be present.

DOCUMENT NUMBER:	98AON23319D	Electronic versions are uncontrolled except when accessed directly from the Document Reposito Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	3.5 MM IPAK, STRAIGHT L	EAD	PAGE 1 OF 1

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DESCRIPTION:	DPAK (SINGLE GAUGE)		PAGE 1 OF 1

STYLE 10:

PIN 1. CATHODE 2. ANODE

3 CATHODE

4. ANODE

STYLE 9:

PIN 1. ANODE 2. CATHODE

3 RESISTOR ADJUST

CATHODE

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STYLE 7: PIN 1. GATE 2. COLLECTOR

3 FMITTER

4. COLLECTOR

STYLE 8:

PIN 1. N/C 2. CATHODE

3 ANODE

CATHODE

STYLE 6:

PIN 1. MT1 2. MT2

3 GATE

device data sheet for actual part marking.

Pb-Free indicator, "G" or microdot "■", may

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