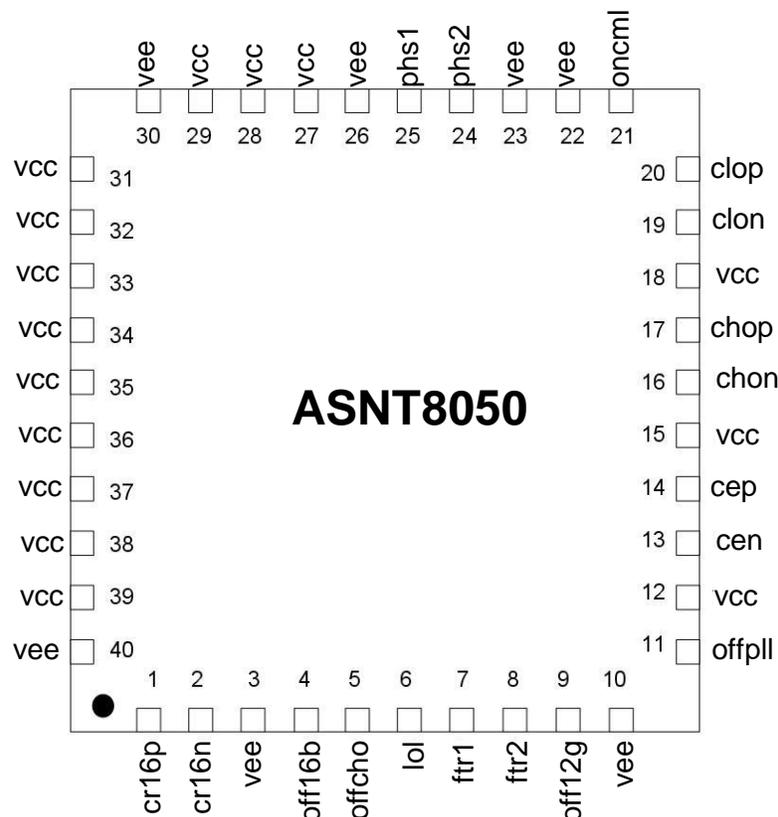# ASNT8050-PQB
7.4-8.8*GHz* and 10.8-12.7*GHz* Programmable PLL with integrated VCOs

- Programmable clock multiplier (CMU) with two selectable frequency ranges of internal PLL

- Optional operational mode as a clock divider with PLL disabled

- Closed-Loop SSB phase noise at 10*MHz* offset better than 98*dB/Hz*

- Selectable internal divider ratio of 8 or 16

- On-chip Loss-of-Lock control circuit

- External RC loop filter

- LVDS or CML input reference clock interface

- Full-rate CML clock input and output interfaces

- LVDS divided clock output with optional 90°-step phase adjustment

- Exhibits low jitter and limited temperature variation over industrial temperature range

- Single +3.3*V* power supply

- Power consumption: 630*mW*

- Fabricated in SiGe for high performance, yield, and reliability
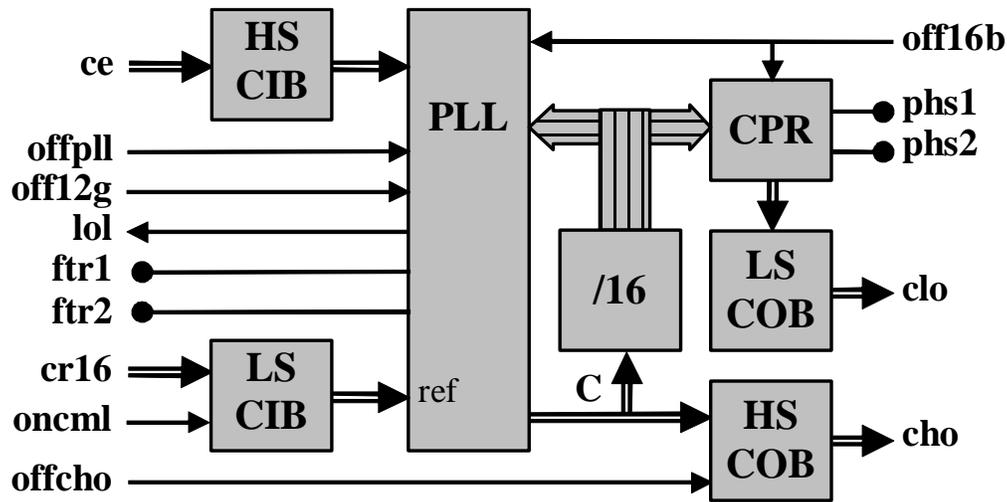
- Standard MLF/QFN 40-pin package

DESCRIPTION

Fig. 1. Functional Block Diagram

ASNT8050-PQB is a clock multiplication unit (CMU) with a dual-range phase-locked loop (PLL) incorporating high-speed voltage-controlled oscillators (VCOs). The part features several control functions shown in Table 1. All functions are further described in the specified sections.

Table 1. PLL Control Functions

Control signal	Logic State			Described in
	"0"	**Not connected (default)**	**"1"**	
off12g	Higher VCO range	Same as "0" state	Lower VCO range	PLL
offcho	HS COB enabled	Same as "0" state	HS COB disabled	HS COB
phs1/phs2	See Table 4			CPR
off16b	Clock division ratio of 16	Same as "0" state	Clock division ratio of 8	PLL, CPR
offpll	PLL enabled	Same as "0" state	PLL disabled	PLL
oncml	LVDS input interface	Same as "0" state	CML input interface	LS CIB

One of the two frequency ranges can be selected by the control signal off12g. In the main operational mode, the IC shown in Fig. 1 accepts a low-speed reference clock cr16p/cr16n with the frequency $f/8$ or $f/16$ and converts it into a high-speed output clock cho with the frequency f and the low-speed output clock clo with the corresponding frequency $f/8$ or $f/16$. The frequency of the reference and output clocks is defined by the settings of the control signal off16b.

The high-speed clock output buffer can be enabled/disabled by the control signal offcho. One of four 90° shifted phases of the low-speed output clock with the frequency $f/16$ can be selected by control signals phs1 and phs2. This phase selection is not available for the output clock with the frequency $f/8$.

When operating in the closed-loop mode, the PLL requires an external loop filter connected to pins ftr1 and ftr2. The output signal lol indicates the locked or unlocked state of the PLL. The PLL also supports an open-loop mode of operation with its selected VCO controlled externally by voltages applied to the filter pins ftr1 and ftr2.

The chip can operate as a divider of the input high-speed clock cep/cen if the PLL is disabled by the control signal offpll. The division ratio of 8 or 16 can be selected by the control signal off16b.

The IC uses a single +3.3*V* power supply and is characterized for operation from −25°*C* to 125°*C* of junction temperature.

HS CIB

The High-Speed Clock Input Buffer (HS CIB) can process an external clock signal cep/cen with frequencies from DC to the specified maximum value. The clock inputs support the CML logic interface with on chip 50*Ohm* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination. In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

LS CIB

The Low-Speed Clock Input Buffer (LS CIB) is a proprietary universal input buffer (UIB) that can run at a high frequency. The UIB's input termination impedance is controlled by the CMOS signal oncml and is set to 100*Ohm* differential if oncml="0" (true LVDS mode, default state) or 50*Ohm* single-ended to vcc if oncml="1" (CML mode). Possible input clock application schemes are detailed in Table 2, where Vcm is the common-mode voltage of the input clock signal.

Table 2. LS Input Clock Application Schemes

Interface type	Clock type	cr16p signal			cr16n signal		
		Swing, *mV*	**Connection**	**Vcm, *V***	**Swing, *mV***	**Connection**	**Vcm, *V***
LVDS (oncml ="0")	Diff.	70-to-500	DC	1.2±1.0	70-to-500	DC	1.2±1.0
	SE	140-to-900	AC	-	Threshold	DC	vee-to-vcc
		Threshold	DC	vee-to-vcc	140-to-900	AC	-
CML (oncml ="1")	Diff.	70-to-500	DC	vcc -Swing/2	70-to-500	DC	vcc-Swing/2
			AC	-		AC	-
	SE	140-to-900	AC	-	-	Not connected	-
		140-to-900	AC	-	Threshold	DC	vcc
		-	Not connected	-	140-to-900	AC	-
		Threshold	DC	vcc	140-to-900	AC	-

As can be seen, the UIB is designed to accept differential signals with DC common mode voltages between the negative (vee) and the positive (vcc) supply rails, as well as AC common mode noise with a frequency up to 5*MHz* and voltage levels from vee to vee+2.4*V*. It can also receive single-ended signals with a threshold voltage between vee and vcc applied to the unused pin of the differential input interface.

PLL

The PLL contains a phase frequency detector, a charge pump, an on-chip integrator with an additional off-chip filter connected between pins ftr1 and ftr2, and two selectable LC-tank VCOs with different central frequencies. The recommended parameters of the external filter schematic components shown in *Fig. 2* are for reference only and can be modified based on specific requirements.
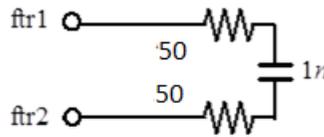
Fig. 2. Recommended External Filter Schematic

The PLL is activated by the external control signal **offpll**="0". In case of **offpll**="1" (default state), the PLL is disabled and the chip operates as a divider by 8 or 16. The division ratio is defined by the CMOS control signal **off16b** (division by 8 if **off16b**="1"; division by 16 if **off16b**="0", default state).

The main function of the PLL is to synthesize the full-rate clock **C** by aligning the phase and frequency of the divided clock from the internal divider to the externally applied reference clock **cr16**. Selection of the required VCO is defined by the CMOS control signal **off12g** (lower-speed VCO if **off12g**="1"; higher-speed VCO if **off12g**="0", default state). The frequency of the required reference clock is defined by the CMOS control signal **off16b** (divided-by-8 if **off16b**="1"; divided-by-16 if **off16b**="0", default state). The state of the PLL is indicated by the output CMOS loss-of-lock alarm signal **lol** (**lol**="1" if PLL is not locked, **lol**="0" if phases and frequencies of internal and reference clocks are matching).

If required, the selected VCO can be externally controlled by voltages applied to the pins **ftr1** and **ftr2** as shown in Table 3. In this case, the PLL is operating in the open-loop mode. The unused VCO is completely disabled to save power.

Table 3. VCO External Control Modes

ftr1 signal, *V*	ftr2 signal, *V*	VCO frequency
Vccm+0.8=3.1	Vccm=2.3	min
Vccm-0.8=1.5	Vccm=2.3	max
Vccm=2.3	Vccm+0.8=3.1	max
Vccm=2.3	Vccm-0.8=1.5	min

Divider-by-16

The Divider-by-16 (/16) includes 4 divide-by-2 circuits connected in series. The clocks divided by 8 and 16 are supplied to the PLL's phase detector and to the clock processor CPR.

CPR

The clock processor (CPR) receives divided clocks from the divider and supplies the selected clock to the low-speed clock output buffer. The type of the clock is defined by the CMOS control signal **off16b** (divided-by-8 if **off16b**="1"; divided-by-16 if **off16b**="0", default state). The phase of the divided-by-16 clock **C16** can be altered utilizing the CMOS control pins **phs1** and **phs2** as shown in Table 4.

Table 4. Output Clock Phase Selection

phs1	phs2	C16 phase
vee (default)	vee (default)	0°
vee	vcc	90°
vcc	vee	180°
vcc	vcc	270°

HS COB

The High Speed Clock Output Buffer (HS COB) receives the high-speed clock from the PLL and converts it into the CML output signal cho. The buffer can be enabled or disabled by the external CMOS control signal offcho (disabled if offcho=”1”; enabled if offcho=”0”, default state).

LS COB

The LVDS Low-Speed Clock Output Buffer (LS COB) converts the signal from the CPR into the LVDS output signal clo. The proprietary low-power LVDS output buffer utilizes a special architecture that ensures operation at frequencies up to $2.0GHz$ with a low power consumption level of $30mW$. The buffer satisfies all requirements of the IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995. For the correct operation, it requires external differential $100Ohm$ DC termination at the receiver side. These pins should **NEVER be CONNECTED** to devices with $50Ohm$ termination to ground **WITHOUT DC BLOCKS!**

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 5 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vee).

Table 5. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vcc)		3.6	*V*
Power Consumption		0.7	*W*
RF Input Voltage Swing (SE)		1.0	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

TERMINAL FUNCTIONS

Name	No.	Type	DESCRIPTION
TERMINAL			DESCRIPTION
High-Speed I/Os			
cep	14	CML input	CML differential external clock inputs with internal SE 50*Ohm* termination to vcc
cen	13		
chop	17	CML output	CML differential clock outputs with internal SE 50*Ohm* termination to vcc. Require external SE 50*Ohm* termination to vcc
chon	16		
Low-Speed I/Os			
cr16p	1	Input	LVDS/CML clock inputs. See *LS CIB* for allowed application schemes
cr16n	2		
clop	20	Output	LVDS clock outputs. See *LS COB* for a detailed description
clon	19		
Controls			
off16b	4	Input	3.3*V* CMOS control signals
offcho	5		
off12g	9		
offpll	11		
oncml	21		
phs2	24		
phs1	25		
ftr1	7	Input	Pins for connecting the external loop filter. Can be also used for VCO external control in the open-loop mode
ftr2	8		
lol	6	Output	3.3*V* CMOS control output

Name	Description	Pin Number
**Supply and Termination Voltages**		
vcc	Positive power supply (+3.3*V*)	12, 15, 18, 27, 28, 29, 31, 32, 33, 34, 35, 36, 37, 38, 39
vee	Negative power supply (0*V*)	3, 10, 22, 23, 26, 30, 40

ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee		0.0		*V*	External ground
vcc	3.1	3.3	3.5	*V*	±6%
*I*vcc	185		195	*mA*	
Power consumption		630		*mW*	
Junction temperature	-40	25	125	*°C*	
HS Input Clock (cep/cen)					
Frequency	DC		14	*GHz*	
Swing	220		800	*mV*	Differential or SE, p-p, at 14*GHz*
	50		800	*mV*	Differential or SE, p-p, at 4*GHz*
CM Voltage Level	vcc-0.8		vcc	*V*	Must match for both inputs
Duty Cycle	40%	50%	60%		
LS Input Clock (cr16p/cr16n)					
Frequency	DC		1600	*MHz*	
Swing	140		900	*mV*	Differential or SE, p-p
CM Voltage Level	vee	1.6	vcc	*V*	Must match for both inputs
HS Output Clock (chop/chon)					
Frequency	DC		14	*GHz*	
Logic "1" level		vcc		*V*	
Logic "0" level		vcc-0.85		*V*	
Jitter		6		*ps*	Peak-to-peak at 12.5*GHz*
Duty Cycle		50%			
LS Output Clock (clop/clon)					
Frequency	DC		1750	*MHz*	
Interface		LVDS			Meets the IEEE Std.
CMOS control inputs and outputs (off16b, offcho, off12g, offpll, oncml, phs1, phs2, lol)					
Logic "1" level	vcc-0.3			*V*	
Logic "0" level			vee+0.3	*V*	
VCOs					
Low frequency of VCO 1		10.8		*GHz*	Higher-speed VCO. Active if **off12g** ="0"
High frequency of VCO 1		12.7		*GHz*	
Low frequency of VCO 2		7.4		*GHz*	Lower-speed VCO. Active if **off12g** ="1"
High frequency of VCO 2		8.8		*GHz*	
External control common mode vccm		2.3		*V*	In the open-loop mode
External control voltage range	vccm-0.8		vccm+0.8	*V*	In the open-loop mode

PACKAGE INFORMATION

The chip die is housed in a standard 40-pin QFN package shown in Fig. 3. It is recommended that the center heat slug located on the back side of the package is soldered to the **vee** plain that is ground for the positive supply.

The part's identification label is ASNT8050-PQB. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.
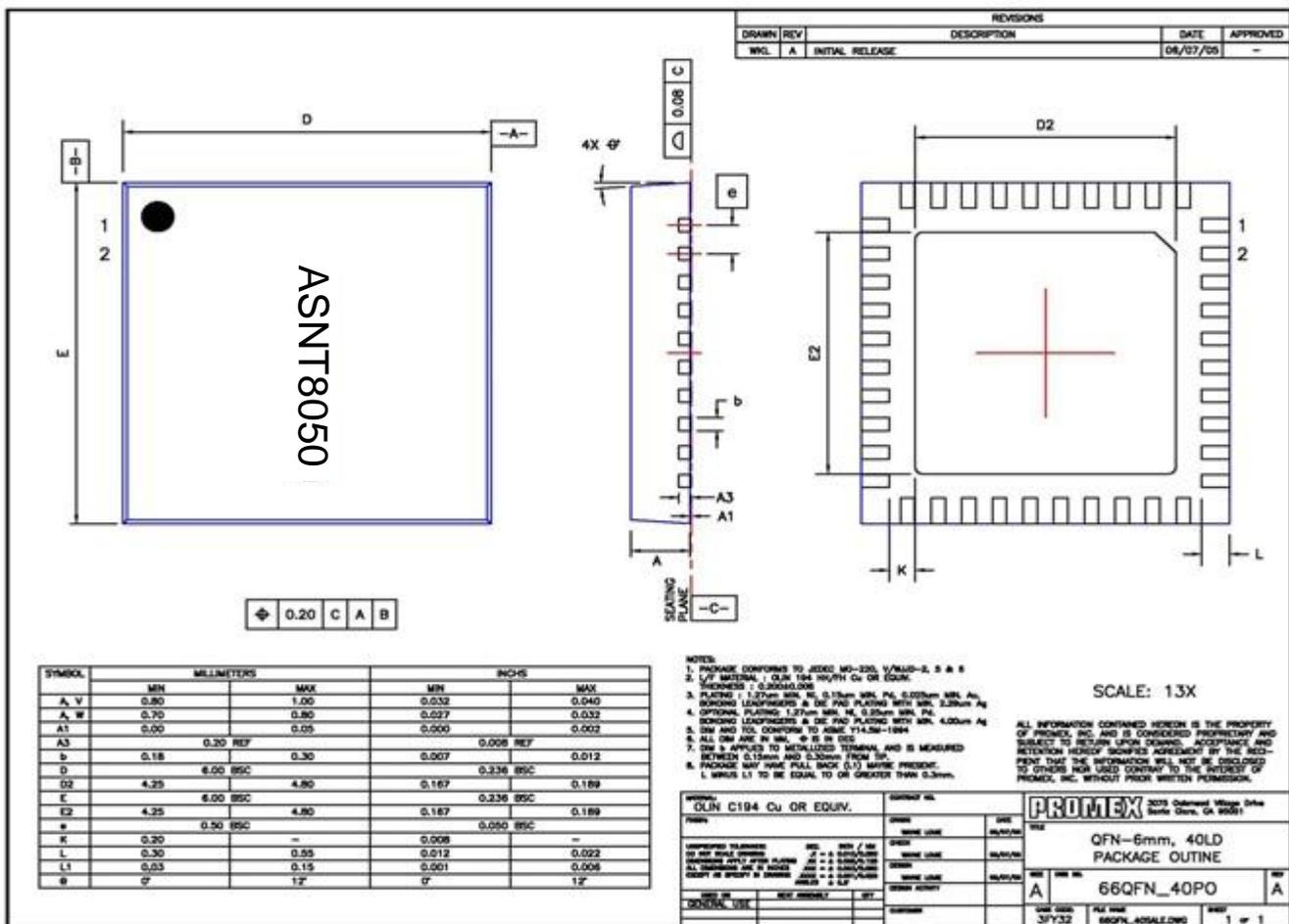

Fig. 3. QFN 40-Pin Package Drawing (All Dimensions in mm)

REVISION HISTORY

Revision	Date	Changes
1.7.2	02-2020	Updated Package Information
1.6.2	07-2019	Updated Letterhead
1.6.1	08-2015	Correct Fig. 2 External Filter Schematic
1.5.1	08-2014	Corrected format Corrected default state of the offpll input
1.4.1	05-2013	Corrected clock names in Table 2
1.3.1	03-2013	Corrected name of the supply in the Absolute Maximum Ratings table Removed broken link
1.2.1	03-2013	Revised title Revised description Revised absolute maximum ratings Revised terminal functions Revised electrical characteristics Revised package information Updated format
1.1	05-2012	Corrected supply information
1.0	04-2012	First release